

Comprehensive AMD Opteron™ Processor (Bulldozer)

Training

Let MindShare Bring AMD Processors to Life for You

The AMD Opteron Processor was the first 64-bit x86-based processor available, implementing the AMD64 instruction set (also known as x86-64). The latest processor family from AMD targeted at the server space is codenamed Bulldozer. These processors are built with multiple Bulldozer "modules," integrated memory controllers, multiple HyperTransport links (Gen3), shared L3 caches, multiple power-planes, etc.

You Will Learn:

- The Bulldozer (Family 15h) microarchitecture
- Basic behaviors of AMD64
- How to optimize code for a Bulldozer-based Opteron processor
- Basic behavior of the BIOS in discovering and initializing multi-socket systems
- Performance implications of AMD's multi-core, multi-socket systems
- Characteristics of the integrated memory controller and effects of a NUMA architecture
- The protocol and features of HyperTransport (Gen1 and Gen3)

Course Length: 4 Days

Course Outline:

- Software Architecture
 - Operating Modes
 - Register Set
 - Segmentation
 - Task Management
 - Interrupts and Exceptions
 - AMD64 Paging Mechanisms
 - Instruction Set Extensions (SSE, SSE2, SSE3, SSE4, SSE4a, SSE5, AVX)
 - Virtualization
- Processor Core Microarchitecture
 - Processor Core Introduction and Terminology
 - Instructions vs Macro-Ops vs Micro-Ops
 - Bulldozer Modules (compute units)
 - The Integer Pipeline
 - Fetch Engine
 - Branch Prediction
 - Scan/Align Logic
 - Instruction Decode
 - Instruction Control Unit
 - Register Renaming
 - Schedulers
 - Execution Units
 - Retirement
 - FPU
 - Register Renaming
 - Scheduling
 - Execution Units
 - Retirement
 - Load/Store Unit
 - The Caches
 - L1 Instruction Cache
 - L1 Data Cache
 - L2 Unified Cache
 - L3 Shared Cache
 - L1 and L2 TLBs

- MOESI Cache Coherency Protocol
- Cache probing example
- System Architecture
 - Example System Topologies
 - System Components on the Chip
 - HyperTransport Overview
 - HyperTransport 1.0
 - HyperTransport 3.0
 - Configuration Space Overview
 - DRAM Technology Overview
 - DDR
 - DDR2
 - DDR3
 - G3MX and FB-DIMM overviews
 - System Power-Up Process
 - BSP Identification and Responsibilities
 - Routing Tables
 - Enumeration I/O Devices
 - HyperTransport Tuning
 - DRAM Address Map
 - NUMA
 - I/O Address Map
 - MMIO Address Map
 - APIC
 - Performance Monitoring Registers
 - Instruction Based Sampling (IBS)
 - Processor Power Management

Recommended Prerequisites: None

Course Materials:

Students will be provided with an electronic version of the slides used in class.

MindShare's *x86 Instruction Set Architecture* Book or eBook

Author: Tom Shanley

Publisher: MindShare Press

