

## Comprehensive Intel 64 and IA-32 (x86) Architecture

### Training

#### Let MindShare Bring Intel 64 and IA-32 to Life for You

Intel 64 is a 64-bit superset of the x86 instruction set architecture. Because the Intel 64 instruction set is a superset of the IA32 (x86) instruction set, all instructions in the x86 instruction set can be executed by CPUs that implement Intel 64; therefore those CPUs can natively run programs that run on x86 processors from Intel, AMD and other vendors. AMD also supports this architecture and refers to it as AMD64 (formerly known as x86-64). This leads to the common use of the names x86-64 or x64 as more vendor-neutral terms to collectively refer to the two nearly identical implementations.

Intel 64 and x86-64 should not be confused with the Intel Itanium architecture, also known as IA-64, which is not compatible on the native instruction set level with the x86 or x86-64 architecture.

#### You Will Learn:

- What the expected behavior of instructions are based on the current operating mode and enabled features
- What the differences are between Intel 64 and AMD64
- How Intel VT (Intel's virtualization technology) alters the behavior of Intel 64 to boost the performance of virtualization solutions

**Course Length:** 3 Days

#### Course Outline:

- x86 Instruction Set Background
- Intro to the Instruction Set
  - General Purpose Instructions
  - Floating Point Instructions
  - Program Flow-related Instructions
  - Hardware-Related Instructions
- Intro to the Register Set and Address Spaces
  - General Purpose registers (GPRs)
  - XMM registers
  - x87 / MMX registers
  - Debug registers
  - Control registers
  - Model-Specific registers (MSRs)
  - REX prefixes
  - Memory, IO, and Configuration Spaces
- Operating Modes
  - Real Mode
  - Protected Mode
  - Virtual-8086 Mode
  - System Management Mode
  - IA32e (Long) Mode
    - 64-bit Mode
    - Compatibility Mode
- Real Mode Operation
- Introduction to Multitasking
- Protected Mode (Segmentation)
  - Privilege Levels (Rings)
  - Code and Data Segment Descriptors
  - Global Descriptor Table (GDT)
  - Local Descriptor Table (LDT)
  - Flat Memory model
- Control Transfers
  - Call Gates

- Optimized System Calls
  - SYSCALL / SYSRET
  - SYSENTER / SYSEXIT
- Automatic Stack Switching
- Task Management
  - Task State Segments (TSS)
  - Task Gates
  - Hardware and Software task switching
- Interrupts and Exceptions
  - Vectors
  - Interrupt priorities
  - Exceptions
  - Interrupt Descriptor Table (IDT)
  - Stack behavior
- Paging Mechanisms
  - Purpose of Paging
  - Paging Basics
  - Physical vs. Virtual (Linear) Address Space
  - TLBs (Translation Lookaside Buffers)
  - Page Size Extensions (PSE)
  - Physical Address Extensions (PAE)
  - IA32e (Long) Mode Paging
  - Execute Disable functionality
- Memory Types
  - Intro to Caches
  - Types
    - UC – Uncacheable (and UC-)
    - WC – Write Combining
    - WP – Write Protect
    - WT – Write Through
    - WB – Write Back
  - Assignment Mechanisms
    - Memory Type and Range Registers (MTRRs)
    - Page Attribute Table Register (PAT)
- Intro to Virtualization Technology (Intel-VT)
- Virtual-8086 Mode

**Recommended Prerequisites:** None

**Course Material:**

MindShare's *x86 Instruction Set Architecture* textbook (1st Edition).

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Available through the MindShare Online Store and major bookstore outlets.

Students will be provided with an electronic version of the slides used in class.