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Comprehensive x86 APIC Architecture

Training

Let MindShare Bring "APICs" to Life for You

This course covers all aspects of the Local and IO APIC modules. This includes the legacy interrupt background, the history of the APIC, a complete description of the operation of the Local and IO APICs, interrupt delivery modes, MSI, and much more.

After taking this course, the attendee will have a full understanding of the APIC's software and hardware operation.

Course Length: 1 Day

Who Should Attend?

This course is intended for hardware and software engineers who require a complete understanding of the Local APIC and IO APIC architecture.

Course Contents:

- Advanced Programmable Interrupt Controllers (APICs)
  - Before APICs
  - Delivery Mechanism to the APIC
  - Enabling/Disabling the Local APIC
  - APIC ID / Cluster ID Assignment
- Interrupt Sources
  - Local Sources
  - Remote Sources
  - User-Defined Interrupts and Priorities
- Local APIC Register Set
- Interrupt Delivery
  - Physical Destination Mode
  - Logical Destination Mode
    - Flat
    - Cluster
- IO APIC
  - Edge-Triggered Interrupts
  - Level-Triggered Interrupts
  - IO APIC Register Set
- In-band Interrupt Messages
  - FSB interrupts
  - Intel QPI Interrupt Messages
  - HyperTransport Interrupt Messages
- Message Signaled Interrupts (MSI)
- Spurious Interrupts

Recommended Prerequisites:

Familiarity with general computer architecture concepts.

Course Material:

MindShare will supply electronic version of the presentation slides.