### MindShare DRAM Quick Reference Guide (Rev 5a)

**DRAM Terms and Glossary  Rev 5a**

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#### 3DS
3 Dimensional Silicon or Stack

ab, AB All Banks (LPDDRs),

AP in PC DDRs

**ACT**
Active aka Activate command

**AL**
Additive Latency, 0 to 5 for DDR2, 0, CL-1, or CL-2 for DDR3 & 4,

**RL** = AL + CL + PL

**AMB**
Advanced Memory Buffer

**AMBA**
Advanced Microcontroller Bus

**AP**
Auto Precharge, Precharge All, A10

**ASR**
Auto Self Refresh, auto temp.,

not Auto Refresh

**AXI**
Advanced eXtensible Interface

**BA**
Bank Address

**BC**
Burst Chop

**BC#**
Burst Chop pin, A12

**BC#**
Burst Chop 4

**BG**
Bank Group

**BGA**
Ball Grid Array

**BL**
Burst Length

**BL4**
Burst Length 4 UI,

inappropriate term for DDR3/4 BC4

**BL8**
Burst Length 8, 8 UI of DQ

**BL9**
Inappropriate term for BL8 + CRC x8,x16

**BL10**
Inappropriate term for BL8 + CRC x4

**C**
Chip ID, like CS# but for 3DS

**Column Address (LPDDR3)**

**CA**
Column Address (DQ)

**CD**
Column Address (DQ)

**CA**
Column Address (DQ)

**CA**
Column Address (DQ)

**CA**
Column Address (DQ)

**CA**
Column Address (DQ)

**CA**
Command and Address (LPDDR3)

**CAS**
Command and Address (LPDDR3)

**CAS**
Command and Address Strobe

**CB**
Check Bit

**CDIMM**
Clocked 72-bit Mini DIMM

**CK**
Clock

**CKE**
Clock Enable

**CL**
CAS Latency (in MR0) = RL – AL

**CRC**
Cyclic Redundancy Check

**CS#**
Chip Select, Rank, # in 21C spec

**CTT**
Center Tap Termination

**CWL**
CAS Write Latency (in MR2)

**DBI#**
Data Bus Inverted

**DES**
Device Deselect (pseudo command)

**DLL**
Delay-Locked Loop

**DDR**
Double Data Rate, DDR1

**DDR1**
Double Data Rate, DDR1

**DDR2**
Double Data Rate, DDR2

**DDR3**
Double Data Rate 3

**DIMM**
Dual In-line Memory Module

**DM**
Data Mask

**DNQ**
Do Not Use, NF, connected on die

**DQ**
Data

**DQS**
Data Strobe

**DRAM**
Dynamic Random Access Memory

**ECC**
Error Checking and Correcting

**eMMC**
Embedded Multi-Media Card

**EMRS**
Extended Mode Register Set

**FBDIMM**
Fully-Buffered DIMM

**FBGA**
Fine-pitch BGA

**GDDR**
Graphics DDR,

not JEDEC DDR1, 2, 3

**HBM**
High Bandwidth Memory

**HSUL**
High Speed Unterminated Logic

**IDD**
I sourced C

**ICH**
Intel IO Controller Hub

**ISM**
Internal Stacked Module

**JEDEC**
Solid State Technology Association,

was Joint Electron Device

Engineering Council

**LDAM**
Lower Data Mask

**LDQS**
Lower Data Strobe

**LP3**
LPDDR3, informally

**LP4**
LPDDR4, informally

**LPDDR**
Low-Power DDR, LPDDR1

**LPDDR2**
Low-Power DDR2

**LPDDR3**
Low-Power DDR3

**LPDDR4**
Low-Power DDR4

**LRDIMM**
Load-Reduced DIMM

**LVSTL**
Low Voltage Swing

**MCH**
Intel Memory Controller Hub

**MCP**
Multi-Chip Package

**MIPI**
Mobile Industry Processor Interface

**MO**
Microelectronic Outline

**MoB**
Motherboard

**M-PHY**
MPI PHY

**MPR**
Multi Purpose Register, NOT a MR

**MR**
Mode Register

**MRR**
Mode Register Read command

**MRS**
Mode Register Set command

**MRW**
Mode Register Write command

**n**
Width of device’s data bus

**n**
One tick of CK as
dimensionless number

**NC**
No Connect, not connected on die

**NF**
No Function, DNU,

connected on die

**ODC**
Off-Chip Driver

**ODT**
On-Die Termination

**OTF**
On The Fly

**PARS**
Partial Array Self Refresh

**PC3**
DD3, informally

**PC4**
DD4, informally

**PCI#**
Intel Platform Controller Hub

**PDA**
Per-DRAM Addressability

**PEC**
SMB Packet Error Checking

**PHY**
Physical Layer

**PL**
Parity Latency

**PLL**
Phase-Locked Loop

**POD**
Pseudo Open Drain

**PoP**
Package on Package

**PRE**
Precharge command

**RA**
Row Address

**RAS**
Row Address Strobe

**RAS**
Reliability, Availability,

Serviceability

**RCR**
RAS-to-CAS Delay

**RCD**
Reduced-Latency DRAM

**RDIMM**
Registered DIMM

**RDQS**
Reduced DQS

**REF**
Refresh command

**RFU**
Reserved for Future Use

**RL**
Read Latency = CL + AL + PL

**RLDRAM**
Reduced-Latency DRAM

**QERR#**
RCD parity error pin

**S#**
CS# in 21C spec

**S3**
Suspend to DRAM pwr mgmt state

**S4EC D4ED**
Single 4-bit Error Correction,

Double 4-bit Error Detection

**SA**
SMB hardware DIMM addr.,

not bused

**SCL**
SMB clock pin, DIMM pin

**SDA**
SMB address and data pin,

DIMM pin

**SDRAM**
Synchronous DRAM

**SECDED**
Single bit Error Correction,

Double bit Error Detection

**SIMM**
Single In-line Memory Module

**SMB**
System Management Bus

**SMBus**
System Management Bus

**SO-DIMM**
Small Outline DIMM

**SPD**
Serial Presence Device or Detect

**SPD ROM**
SPD ROM

**SRAM**
Static Random Access Memory

**SRT**
Self Refresh Temperature, see ASR

**SSTL**
Stub Series-Terminated Logic

**T**
1T, 2T, 3T, etc. timing,

as 1N, 2N, etc.

**tCK**
Time for one tick of CK

**tXXX**
JEDEC timing spec XXX

**TDQS**
Termination DQ, not RDQS

**TSOP**
Thin Small Outline Package

**TSS**
Through Silicon Via

**TUF**
Temperature Update Flag

**UDIMM**
Unbuffered DIMM

**UDM**
Upper Data Mask

**UDQ**
Upper Data Strobe

**UFSS**
Universal Flash Storage

**UFS**
Universal Flash Storage Association

**VCC**
Core Power

**VDD**
Power (not for DRAM)

**VREF**
Reference Voltage

**VPD**
Voltage Pump Replacement Power

**VSS**
Ground

**VTT**
Termination Voltage

**VLP**
Very Low Profile

**WCL**
Write Command Latency (not CWL)

**WL**
Write Latency

1 for DDR1; RL - 1 for DDR2;

variable for DDR3 & DDR4

**XDR**
Rambus DRAM,

improperly ‘XDRAM’

**ZQ**
Data Source Impedance:

Q=Data, Z=impedance

#### Numbering

1n, 2n, 4n, 8n  Prefetch widths

1T, 1N  New command every clock

2T, 2N  New command every other clock

4T, 4N  Variable for DDR3 & 4

**DDRn-mmm**  n=2,3,4 mmm=MT/s

Example: DDR2-800 = 400MHz CK

**PC 97**, **PC 99**  Microsoft PC requirements,

not DRAM

**PC 100**  Early SDRAM DIMM bandwidth

**PCn-xxxx**  xxx=x=DDIMM KB/sec bandwidth

=MT/s × DIMM data width / 8

**x-x-x**  CL=8, 23, 4 mmm=MT/s

**x-x-x-x**  CL=8, 23, 4 mmm=MT/s

n × n × n  Array density × data width × #banks

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Terms

Access time CK to DQS.
Formerly RAS# to valid data

Activate ACT Active Command

Active ACT Active Command, Open

Array One bank of the device

Auto Precharge Precharge after read/write
w/o explicit PRE cmd.

Auto Refresh Just Refresh,
not ASR nor Self Refresh

Bank Formerly rank.
Internal to DRAM device.

Bank Group Four banks in DDR4

Bit Line Several per column

Burst Sequential or interleaved

Channel Interface between controller's
PHY and a rank of DRAM;
SMB & SPD are not on the
channel.

Column In Read/Write command
Command RAS#, CAS#, and WE#

Control CS#, CKE, and ODT

Data Group DQ, DQS, DM/DBI

Dynamic ODT ODT when written to.

Fast CKE Power Down Power Down w/ DLL
Enabled

Idle Closed, Precharged

Open Active, Activated

Page Row

Page size Row size expressed as bytes
not bits

Postamble DQS after read/write

Preactive NVM term, NOT DRAM

Preamble DQS before read/write

Precharge PRE/PREA command

Prefetch width 1n, 2n, 4n, 8n, 16n

Rank CS#

Raw Card JESD21C DIMMs

Refresh Auto Refresh

Registered Sampled, latched

Row In ACT command

Self Refresh In ACT command

Word Line One per row

Write Leveling DDR3/4 write DQS calibration

Write Levelization Write Leveling

Commands

ACT Bank ACTive aka ACTivate

BST Burst Terminate, Burst STOP

DES Device DESSelect, CS# false

DPD Deep Power Down entry

DPDX Deep Power Down eXit

EMRS Extended Mode Register Set

MRR Mode Register Read

MRS Mode Register Set

MRW Mode Register Write

NOP No Operation

PD Power-Down entry

PDE Power-Down Entry

PDX Power-Down eXit

PR Per-bank Precharge

PRA All-bank Precharge

PRE Single-bank PREcharge

PREA PPREcharge All banks

RD RealD fixed BL8 or BC4

RDA RD w/Auto-precharge

RDAS4 RDA BC4, OTF

RDAS8 RDA BL8, OTF

RD54 RD BC4, OTF

RD58 RD BL8, OTF

REF REFresh

SRE Self-Refresh Entry

SREF Self-REFresh entry

SREFX Self-REFresh eXit

SRX Self-Refresh eXit

WR WRite fixed BL8 or BC4

WRA WR w/Auto-precharge

WRAS4 WRA BC4, OTF

WRAS8 WRA BL8, OTF

WRS4 WR BC4, OTF

WRS8 WR BL8, OTF

ZQCL ZQ Calibration Long

ZQCS ZQ Calibration Short

Timings

\( t_{AA} \) Time internal read to first data

\( t_{AC} \) Time CK to DQS, access

\( t_{CH} \) Time CK high

\( t_{CK} \) Time CK period

\( t_{CL} \) Time CK low,

\( t_{DQSCK} \) Time CK to DQS

\( t_{FAW} \) Time Four Activate Window

\( t_{RC} \) Time ACT to ACT or ACT to REF,

max 9 x \( t_{REFI} \), min by speed bin

\( t_{RCD} \) Time RAS-to-CAS delay,

ACT to RD/WR

\( t_{RDP} \) Time Precharge, Recovery Period

\( t_{RP} \) Time Precharge, Recovery Period

\( t_{RTP} \) Time Read to Precharge

\( t_{XX} \) as in \( t_{CK} \), time period,
inconsistently used as in \( t_{CCD,S}=5 \),
which is 5 ticks, not 5ns.

\( n_{XX} \) as in \( n_{RCD} \), number of CK ticks,
inconsistently used as in \( t_{AA}+2nCK \),
which should be \( t_{AA}+2t_{CK} \).

\( CL = \) ticks for CAS Latency,
never shown as nCL.

Specifications

JESD8-8 SSTL_3 3.3 volt spec

JESD8-9B SSTL_2 2.5 volt spec

JESD8-15A SSTL_1 1.8 volt spec

JESD8-18A FBDIMM signals (not SSTL_18)

? SSTL_15 1.5 volt spec

JESD8-22 HSUL spec

JESD8-24 1.2v POD spec

JESD21C DIMM (and thus SPD) spec

JESD79F DDR SDRAM standard

JESD79-2F DDR2 SDRAM standard

JESD79-3F DDR3 SDRAM standard

JESD79-3-1DDR3L SDRAM standard

JESD79-3-2DDR3U SDRAM standard

JESD79-4 DDR4 SDRAM standard

JESD209B LPDDR1 SDRAM standard

JESD209-2E LPDDR2 SDRAM standard

JESD209-3B LPDDR3 SDRAM standard

JESD229 Wide IO SDRAM standard

MO-207 BGA package spec

MO-309A DDR4 DIMM spec

Signal Suffixes

# asserted low, negative logic

# complementary signal in
differential pair

_n asserted low, negative logic

t true signal in differential pair

c complementary signal in
differential pair

r rising

f falling