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ARM 64-bit v8A Processor-Based Server SoC Architecture

Training

Let MindShare Bring "ARM 64-bit v8A Processor-Based Server SoC Architecture" to Life for You

This course describes the architecture of ARM's 64-bit processors and SoC architecture. Examples of SoCs that implement this 64-bit architecture are the ARM Cortex-A53 and Cortex A57 processors. The courses covers the ISA (Instruction Set Architecture) details, pipeline information for some implementations of the v8A architecture, interconnect details, cache management, and power management.

You Will Learn:

- ARM architecture (ARMv8-A)
- 64-bit ISA (registers, instruction set etc)
- Memory and paging architecture
- Exception and Interrupt handling
- Pipeline implementations
- Cache management
- System interconnects
- Power management
- Server specific SoC features

Course Length: 4-Days, with optional additional modules

Target Audience:

This course is aimed at SoC design engineers, validation engineers, and software developers and system architects developing for systems powered by ARMv8-A processors such as Cortex-A53 and Cortex-A57 processors. It is relevant for operating system development, device drivers, low-level coding and for application software.

Course Outline:

- Introduction to ARM 64-bit Architecture
- ARM architecture profiles, what is v8-A
- v8-A introduction and rational
- Support for v7 legacy code
- 64-bit platform architecture overview
    - Sample SoC
- A64 ISA introduction
- Integer registers
- Instruction set
    - Integer operations
    - Memory operations
    - Stack
    - System instructions
        - System control registers
        - Relationship to v7 support and co-processors
    - Calling conventions
    - Memory access (DRAM and device)
        - Memory mapped access to devices
        - Memory types

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        - Ordering model
        - Barriers
            - dmb, dsb, isb
            - load-acquire and store-release
            - Domains
        - Semaphores
        - Cache management
    - Floating point, advanced SIMD, crypto
        - Registers and instructions
    - Exception levels
        - The 4 exception levels
        - Stack model, handler and thread
        - Vector table
        - Core implementation choices
        - Switching AArch32 and AArch64 state
    - Exception and interrupt handling
        - Control of delivery of exceptions and interrupts
        - Syndrome registers
        - Switching exception levels
        - Return from exception
    - Paging
        - Page tables
        - 4K, 16K and 64K granules
        - Page sizes, support for large pages
        - TLB management
- Caches
    - Cache architecture
    - Multiple cache levels
    - Instruction and data/unified caches
    - Hardware cache coherency, MP Core and multi-cluster
    - Shareability domains
    - I/O cache coherency
    - Software responsibilities
    - Cache control
- Security (TrustZone)
    - Trustzone overview
    - Switching bitness of TrustZone between 32-bit and 64-bit
- Virtualization overview
- ARM Piplelines
    - Cortex-A57
- Interconnects and multi-core support
    - MP Core
    - Role of the interconnect
    - Cache oherency and the interconnect
    - DVM and the interconnect
    - Role of the interconnect in memory ordering models
    - CHI
- Interrupt architectures
    - Interrupt delivery across multiple cores
    - Software generated interrupts
    - Interrupt controller
    - Memory mapped interrupts
- Firmware
    - Booting
    - UEFI overview
    - ACPI overview

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- PCIe support
  - Bridge to PCIe
  - Interrupt delivery
  - Configuration space
- Other topics
  - Core power management, power controller
    - Power modes (dormant, shutdown)
    - WFI, WFE, SEV
  - Server reliability features, ECC protection, error reporting
  - Debug
  - Linaro
  - 64-bit tool chain overview
  - 64-bit Linux overview

Optional Topics (Not covered in standard 4-day course)

- 32-bit v7 Architecture Overview **(1-day)**
  - Overview of 32-bit v7 ISA (registers, instruction set, etc.)
  - Memory and Paging architecture overview
  - Interrupt handling and exception overview
  - Floating Point, TrustZone and NEON overview
  - Example 32-bit processor pipeline overview
- Additional 64-bit ISA material not covered in standard 4-day course **(1 day)**
- ARM processor virtualization support **(1-day)**
  - Processor mode (Hyp mode, EL2) added in 32-bit ARM to implement hardware virtualization of the processor core
  - The intersection of virtualization support and security support (TrustZone)
  - ARM 64-bit processor virtualization implementation – Exception Levels 2 and 3
  - Interrupts and Virtualization
  - Memory management
  - Paravirtualization techniques
  - Hardware support for paging guest operating systems
  - Significance of guest physical (intermediate physical address space), especially with regard to I/O
  - The SMMU
  - TLB management and TLB features to support virtualization
  - IO Virtualization

Recommended Prerequisites:

Prior knowledge of ARM 32-bit v7 architecture is assumed.

Course Materials:

Students will be provided with an electronic version of the slides used in class.