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ARMv8-M Architecture

Training

Let MindShare Bring "ARMv8-M Architecture" to Life for You

This course covers the addition of ARMv8-M to the existing v7-M and v6-M architectures. Examples of processors that implement ARMv8-M architecture are ARM Cortex-M23 and Cortex M33 processors. Additional processors are in development. The course covers Instruction Set Architecture (ISA) details including TrustZone security extensions. We also discuss AMBA5 bus architecture and pipeline designs for Cortex-M23 and –M33 processors.

You Will Learn:

- ARM's v8-M architecture.
- The relationship to other ARM architectures.
- The changes from the earlier v6-M and v7-M architectures.
- The security extensions new in v8-M (TrustZone).
- The optional FPU and DSP extensions.
- Platform and tools overview.

Course Length: 4-Days.

Target Audience:

This course is aimed at software developers and system architects developing for systems powered by ARMv8-M processors, such as the Cortex-M23 and the Cortex-M33 processors. It is relevant for operating system development, device driver development, low-level coding and security firmware, and for validation and debug.

Course Outline:

- Introduction to ARM Architecture
  - Introduction to ARM, business model, history, products and architectures
- Overview
  - Architecture background, v6-M, V7-M, v8-M Baseline, v8-M Mainline
  - Platform overview
  - Processor overview
  - ISA introduction, instructions, memory
  - Terminology changes
- ARMv8-M Architecture (combined Baseline and Mainline)
  - Instructions, load/store, data processing, system
  - Execute only support (movw, movt, readonly data sections)
  - Privilege
  - Memory
    - memory map
    - shareability
    - cacheability
    - memory ordering and barriers (isb, dmb, dsb)
    - writing code compatible with other ARM architectures
    - semaphores (ldrex and strex)
    - local and global monitor
    - load acquire, store release
    - device memory (gathering and reordering and early acknowledgement)
    - memory protection (PMSA)
    - stack, stack alignment, and stack limit

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    - Exceptions
        - Exception model, exception entry and exit behavior
        - Handler mode, thread mode, mode switching, and stacks
        - Prioritization and control
        - Vector table
        - Nested Vectored Interrupt Controller
        - NMI
        - Interrupt delivery by microcode, writing handlers in C
        - Exception return
        - Nested interrupts, tail chaining
        - Internal exceptions, SysTick, SVC, PendSV
        - Fault Exceptions
        - Lockup
        - Interruptible instructions
        - Reset
    - DSP extension
    - FPU extension
    - Incompatibilities from v6-M, v7-M
- Tools Overview
    - Calling conventions
    - ARM compiler v 6
    - CMSIS
- Debug Overview
    - ARM Fast Models (simulation, instruction accurate)
    - ARM Cycle Models (simulation)
    - ITM
    - MTB
    - ETM
    - TPIU
    - CTI
    - BPU (no flash patch)
    - DWT
- AMBA5 Overview
    - Platform
    - AHB
- Optional Security Extension (TrustZone for v8-M)
    - Review of v8-A TrustZone to identify the differences
    - v8-M TrustZone big picture
    - Banked registers.
    - Stacks, hardware saved stack frames, integrity signature
    - Floating point in secure world, Lazy floating point stacking
    - Calling between normal world and secure world.
    - Secure memory, normal memory, non-secure-callable memory
    - bxns blxns sg tt instructions
    - Secure fault
    - NVIC and secure control
    - Exceptions and switching worlds, hardware saved state
    - Exception return
    - Exception priorities
    - Chaining exceptions
    - Interrupt latency
    - SAU and IDAU, and memory protection units
    - Bus and platform support
    - Secure firmware
    - Compiler support (execute only permissions)
- ARM Implementations Overview
    - Cortex-M23 (derivative of M0+).

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    - Overview, and architecture (v8-M Baseline)
    - Configuration options
    - Interfaces
    - Debug support
    - Pipeline and execution
- Cortex-M33 (derivative of M4)
    - Overview and architecture (v8-M Mainline)
    - Configuration options
    - Interfaces
    - Debug support
    - Pipeline and execution

Recommended Prerequisites:

Background in computer architecture and processor design.

Course Materials:

Students will be provided with an electronic version of the slides used in class.