1-512-256-0197
www.mindshare.com
training@mindshare.com

ARMv7 32-bit Architecture

Training

Let MindShare Bring "ARMv7 32-bit Architecture" To Life For You

The ARMv7 32-bit Architecture course focuses on software-related aspects of the ARMv7 Architecture, with a specific focus on Cortex-A and Cortex-R profiles, plus common subjects like software tools. This course is aimed at embedded software and systems developers who would like to acquire a broad knowledge of ARM technology with a bias toward application processors and real-time processors.

This course was endorsed by ARM for anyone wanting to take the ARM Accredited Engineer (AAE) certification exam when ARM was still offering their AAE certification program. That program has been discontinued by ARM, but the information in this course is still very relevant and extremely valuable for anyone working with ARM v7 architectures.

ARM Endorsement

"On the strength of MindShare's position as an industry leader in technology training, particularly in the area of microprocessor architecture, we were happy to welcome them to the AAE program as an ARM Accreditation Training Partner (AATP). Their expertise in delivering engaging self-paced eLearning courses should make MindShare's ARM Accredited Engineer Certification eLearning course a very good way to efficiently and cost-effectively prepare for the ARM Accredited Engineer (AAE) exam".
- Daniel Dearing, AAE Program Manager

You Will Learn:

- ARM processor architecture (v5,v6,v7,v8)
- ARM architecture registers
- ARM instructions and syntax
- Interrupt handling environment
- Memory architecture, paging and caches
- ARM virtualization
- About various ARM processor flavors (-M, -A, -R)
- AMBA buses
- Boot processes
- Software development and code optimization

Course Length: 3 Days

Course Outline:

- ARM Introduction
  - Intro to ARM the company
- Sample SoCs and Multiple Processor Cores
  - Descriptions of several common ARM-based SoCs and goes over the concepts of multiple cores and multi-processing (SMP vs. AMP)
- ARM Processor Architectures
  - ARM architecture evolution (v5, v6, v7 and v8) as well as the architecture profiles (-A, -R and -M)
- Architecture Introduction
  - Overview of the instruction sets supported and introduces the concepts of privilege levels and exception levels
- Integer Registers

1-800-633-1440
www.mindshare.com
training@mindshare.com

  - Integer registers of the ARM architecture, the purpose and behavior of register banking and the Program Status Register
- Instructions - ARM
  - ARM assembler syntax, numerous data processing instructions including some on bit manipulation as well as saturation effects
- Instructions - ARM
  - Branch, conditional branch and branch/link instructions as well as how condition codes on instructions behave
- Instructions - Thumb/2, Jazelle, VZP and Neon
  - Differences between ARM and Thumb/Thumb2 instructions and then goes through several examples of conditional execution in Thumb (If/Then/Else); Jazelle, Vector Floating Point and Neon instructions are also discussed at a high level
- Memory Accesses
  - Alignment of memory accesses, endianness and numerous LDR/STR addressing examples including a discussion on pre- versus post-indexing; memory copy examples are also covered
  - Supported memory types and then goes through access ordering, several memory barrier examples, a semaphore synchronization example as well as the behavior of self-modifying code; Shareability domains are also covered
- Privilege, Modes, State, TrustZone and more
  - Privilege Levels, the basic processor modes, provides an overview of TrustZone, the implemented virtualization extensions, and the concept of coprocessors
- Exceptions and Interrupts
  - Exceptions and interrupts including some info on common interrupt controllers
- Memory Management and Protection
  - Memory management behavior typical in the -M profile as well as the memory protection scheme commonly used in the -R profile
- Paging
  - Introduction to managing and protecting memory using paging (typical in -A profile), includes a discussion of TLBs and their management
- v7 LPAE and Hardware Virtualization
  - Implementation of large physical addresses in the v7 architecture as well as the effects of hardware virtualization on paging
- Debug and Analysis Support
  - Different levels of debug that can be used and how each works
- Caches
  - Caching, including cache line states, coherency and cache policies; Then shows Cortex-A9 caches as an example
- The Different Processor Cores
  - Overview of some of the older ARM processor families, including descriptions of their instruction pipelines
- Cortex-M0/1/3/4 and Cortex-R4/5
  - Feature set and instruction pipelines of the Cortex-M0, Cortex-M0+, Cortex-M3/-M4 as well as the Cortex-R4 and Cortex-R5
- Cortex-A8/9/5
  - Feature set and instruction pipelines of the Cortex-A8, Cortex-A9 and Cortex-A5
- Cortex-A15/7/12
  - Feature set and instruction pipelines of the Cortex-A15, Cortex-A7 and Cortex-A12
- AMBA - The Buses
  - AMBA 3, AMBA 4 as well as AXI and the coherency extensions added to this interconnect
- Power Management and Booting
  - Intro to power management on ARM-based systems as well as a generic boot process
- Software Development

  - Overview of the software development process which includes a discussion of the purposes of the compiler and linker as well as object files, libraries (static vs dynamic) and the ARM ABI (Application Binary Interface)
- Software Optimization
  - Optimization as well as the order of effort applied for code optimization; Includes topics such as: pointer aliasing, loop termination, parameter passing, compiler options, inline examples, variable types, data layout and packing of structures, base pointer optimization and more. Also briefly touches on some profiling tools and what they are useful for.

Recommended Prerequisites:

Knowledge of basic computer architecture is recommended.

Course Material:

Students will be provided with an electronic version of the slides used in class.