

Compute Express Link (CXL) Architecture

Let MindShare Bring “Compute Express Link (CXL) 2.0 Architecture” to Life for You

Compute Express Link (CXL) is a high-bandwidth, low-latency serial bus interconnect between host processors and devices such as accelerators, memory controllers/buffers, and I/O devices. CXL is based on PCI Express® (PCIe®) 5.0 physical layer running at 32 GT/s with x16, x8 and x4 link widths. Degraded modes run at 16 GT/s and 8 GT/s with x2 and x1 link widths.

CXL interconnect adds coherency and memory semantics, thus allowing for its application in heterogeneous processing systems with a variety of host processors, memory subsystems and peripheral devices interconnected. CXL has applications in standard computer systems, Artificial Intelligence, Machine Learning, communication systems, and High Performance Computing. Emerging applications require a diverse mix of CPUs, GPUs, FPGAs, peripherals such as smart NICs, and other accelerators interconnected via an open industry standard protocol with the necessary features which CXL provides. CXL provides a rich set of three protocols that include 1) CXL.io based on PCIe, 2) CXL.cache and 3) CXL.mem semantics. CXL uses the PCIe stack offering full interoperability with PCIe.

MindShare’s comprehensive CXL 2.0 Architecture course provides a solid foundation of platform architectures and use cases of the three CXL protocols with Type 1, Type 2 and Type 3 devices. The course then details the role of the Transaction Layer, Link Layer, ARB/MUX and Flex Bus Logical and Electrical Physical Layer of a CXL port design. We explain enumeration and configuration process during system bring-up with details of configuration registers. Other topics include: switch architecture, reset, manageability, RAS features, power management, performance considerations and compliance testing.

You Will Learn:

- CXL system architectures with Type 1, Type 2 and Type 3 devices
- CXL transaction protocol for CXL.io and CXL.cache/mem
- CXL port design constituting Transaction, Link, ARB/MUX and Flex Bus Physical Layers
- CXL switch architecture (optional topic)
- Enumeration and initialization issues with configuration register definitions
- Power management
- Reliability, Availability, Serviceability (RAS) and error handling features
- Considerations to improve protocol performance

Course Length: 4 Days (5-day with CXL Switch Architecture)

Course Outline:

- CXL Features and Architecture Overview
 - Limitations of interconnects that do not support coherency and memory semantics
 - CXL and Flex Bus Link features
 - CXL.io, CXL.cache, CXL.mem
 - Type 1 (devices with cache), Type 2 (devices with memory) and Type 3 (memory expander with no compute engine) devices
 - Layered architecture overview
 - Transaction flows for PCIe, Type 1, 2 and Type 3 devices
 - Cache coherency and MESI protocol tutorial

- CXL Transaction Layer
 - CXL.mem protocol
 - CXL.cache protocol
 - CXL.io protocol
 - Ordering rules
- CXL Link Layer
 - CXL.io Link Layer
 - CXL.cache and CXL.mem common Link Layer
 - CXL.io and CXL.cache/mem Flit packets
 - Link Layer initialization
 - Flow control
 - CXL.cache/CXL.mem retry mechanism
 - Viral feature
- CXL ARB/MUX Layer
 - Arbitration and Data Multiplexing/Demultiplexing feature
 - Virtual Link State Machine (vLSM) states
 - ARB/MUX Link Management packets
- Flex Bus Physical Layer
 - Protocol ID
 - NULL Packets
 - Byte Striping
 - Link training
 - Latency Optimized (Sync Header Bypass) mode
- Resets
 - Cold reset
 - Warm reset
 - Hot Reset
 - Function Level reset (FLR)
 - CXL Reset
- Power Management
 - Runtime control power management
 - Physical Layer power management
 - CXL.io power management
 - CXL.cache + CXL.mem power management
- RAS and Error Handling
 - RAS features
 - Error handling
 - Viral handling
 - Error injection
- Enumeration and Manageability
 - Memory Interleaving
- Registers
 - Configuration and Status registers including RCRB registers and DVSEC registers
 - Memory Mapped registers including MEMBAR0/Component registers
- Performance Considerations

Optional Topics (Extra 1-day)

- CXL Switch Architecture
 - Architecture overview with configuration options
 - CXL.io and CXL.cache/mem transaction decoding and forwarding
 - Switch power management
 - Switch RAS (error handling)
 - Fabric Manager API to switch and Event Records



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Recommended Prerequisites:

Good working knowledge of PCI Express a must. Computer architecture fundamentals. Knowledge of Intel, AMD or Arm processor architectures.

Course Material:

- 1) Downloadable PDF version of the presentation slides
- 2) Optional CXL 2.0 eLearning course



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