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# Compute Express Link (CXL) Architecture

## Let MindShare Bring "Compute Express Link (CXL) 2.0 Architecture" to Life for You

Compute Express Link (CXL) is a high-bandwidth, low-latency serial bus interconnect between host processors and devices such as accelerators, memory controllers/buffers, and I/O devices. CXL is based on PCI Express® (PCIe®) 5.0 physical layer running at 32 GT/s with x16, x8 and x4 link widths. Degraded modes run at 16 GT/s and 8 GT/s with x2 and x1 link widths.

CXL interconnect adds coherency and memory semantics, thus allowing for its application in heterogeneous processing systems with a variety of host processors, memory subsystems and peripheral devices interconnected. CXL has applications in standard computer systems, Artificial Intelligence, Machine Learning, communication systems, and High Performance Computing. Emerging applications require a diverse mix of CPUs, GPUs, FPGAs, peripherals such as smart NICs, and other accelerators interconnected via an open industry standard protocol with the necessary features which CXL provides. CXL provides a rich set of three protocols that include 1) CXL.io based on PCIe, 2) CXL.cache and 3) CXL.mem semantics. CXL uses the PCIe stack offering full interoperability with PCIe.

MindShare's comprehensive CXL 2.0 Architecture course provides a solid foundation of platform architectures and use cases of the three CXL protocols with Type 1, Type 2 and Type 3 devices. The course then details the role of the Transaction Layer, Link Layer, ARB/MUX and Flex Bus Logical and Electrical Physical Layer of a CXL port design. We explain enumeration and configuration process during system bring-up with details of configuration registers. Other topics include: switch architecture, reset, manageability, RAS features, power management, performance considerations and compliance testing.

## You Will Learn:

- CXL system architectures with Type 1, Type 2 and Type 3 devices
- CXL transaction protocol for CXL.io and CXL.cache/mem
- CXL port design constituting Transaction, Link, ARB/MUX and Flex Bus Physical Layers
- CXL switch architecture
- Enumeration and initialization issues with configuration register definitions
- Power management
- Reliability, Availability, Serviceability (RAS) and error handling features
- Flex Bus connector and AIC form factors
- Considerations to improve protocol performance
- Methodology for ensuring device compliance to CXL specification

## Course Length: 4 Days

## Course Outline:

- CXL Features and Architecture Overview
  - Limitations of interconnects that do not support coherency and memory semantics
  - CXL and Flex Bus Link features
  - CXL.io, CXL.cache, CXL.mem
  - Type 1 (devices with cache), Type 2 (devices with memory) and Type 3 (memory expander with no compute engine) devices
  - Layered architecture overview

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- CXL Transaction Layer
  - CXL.io protocol
  - CXL.cache protocol
    - Cacheability
  - CXL.mem protocol
  - Transaction flows for Type 1, 2 and Type 3 devices
- CXL Link Layer
  - CXL.io Link Layer
  - CXL.cache and CXL.mem common Link Layer
  - Flit packets
  - Link Layer initialization
  - CXL.cache/CXL.mem retry mechanism
  - CXL.cache viral feature
- CXL ARB/MUX Layer
  - Virtual Link State Machine (vLSM) states
  - ARB/MUX Link Management packets and Bypass feature
  - Arbitration and Data Multiplexing/Demultiplexing feature
- Flex Bus Physical Layer
  - Framing and packet layout
  - Link training
  - Retimers and low-latency mode
- CXL Switch Architecture
  - Architecture overview with configuration options
  - CXL.io and CXL.cache/mem transaction decoding and forwarding
  - Switch power management
  - Switch RAS (error handling)
  - Fabric Manager API to switch and Event Records
- Registers
  - Configuration and Status registers including RCRB registers
  - Memory Mapped registers including RCRB registers
- Resets
  - Boot flow
  - Cold reset
  - Warm reset
  - Function Level reset (FLR)
- Enumeration and Manageability
- Power Management
  - Runtime control power management
  - Physical Layer power management
  - CXL.io power management
  - CXL.cache + CXL.mem power management
- RAS and Error Handling
  - RAS features
  - Error handling
  - Link Down handling
  - Viral handling
  - Error injection
- Connectors
  - Flex Bus connector
  - AIC form factor
  - Flex Bus slot auxiliary power
- Performance Considerations
- CXL Compliance Testing Overview

## Recommended Prerequisites:

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Basic understanding of serial bus architectures such as PCI Express or QuickPath Interconnect. Computer architecture fundamentals. Knowledge or Intel or AMD processor architectures.

## Course Material:

Downloadable PDF version of the presentation slides