1-512-256-0197
www.mindshare.com
training@mindshare.com

Compute Express Link (CXL) Architecture Fundamentals

Let MindShare Bring "Compute Express Link (CXL) Fundamentals" to Life for You

Compute Express Link (CXL) is a high-bandwidth, low-latency serial bus interconnect between host processors and devices such as accelerators, memory controllers/buffers, and I/O devices. CXL is based on PCI Express® (PCIe®) 5.0 physical layer running at 32 GT/s with x16, x8 and x4 link widths.

CXL interconnect adds coherency and memory semantics, thus allowing for its application in heterogeneous processing systems with a variety of host processors, memory subsystems and peripheral devices interconnected. CXL has applications in standard computer systems, Artificial Intelligence, Machine Learning, communication systems, and High Performance Computing. Emerging applications require a diverse mix of CPUs, GPUs, FPGAs, peripherals such as smart NICs, and other accelerators interconnected via an open industry standard protocol. CXL provides a rich set of three protocols that include 1) CXL.io based on PCIe, 2) CXL.cache and 3) CXL.mem semantics. CXL uses the PCIe stack offering full interoperability with PCIe.

MindShare's CXL Fundamentals course provides a solid foundation of platform architectures and use cases of the three CXL protocols with Type 1, Type 2 and Type 3 devices. Engineering managers will learn about features and capability of each of the three device types allowing decision making about type of device to implement.

You Will Learn:

- CXL features and architecture of Type 1, Type 2 and Type 3 devices
- What is new with CXL 2.0
- CXL switches and MLD device overview
- CXL port design overview: Transaction, Link, ARB/MUX and Flex Bus Physical Layers
- Organization of Control and Status register space

Course Length: 1 Day (2 Half-Days)

Who Should Attend?

Engineering managers and designers looking to understand basic features and capabilities of CXL.

Course Outline:

- CXL Features and Architecture Overview
  - Limitations of interconnects that do not support coherency and memory semantics
  - What are CXL.io, CXL.cache, CXL.memory protocols
  - Type 1 (devices with cache), Type 2 (devices with cache and memory) and Type 3 (memory expander with no compute engine) devices and their use cases
- Overview of the function of each layer of a CXL port
  - Transaction Layer
  - Link Layer
  - Arb/Mux Layer
  - Physical Layer
- Control and Status Register space organization

Recommended Prerequisites:

Basic understanding of computer architecture and any serial bus architectures such as PCI Express.

Course Material:

Downloadable PDF version of the presentation slides