1-512-256-0197
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Comprehensive DRAM (DDR5/LPDDR5) Architecture Course Info

Let MindShare Bring "DRAM (DDRx/LPDDRx) Architecture" to Life for You

Whether you are new to DRAM or an industry veteran seeking the latest and greatest standards, you will learn more than you expect from MindShare's DRAM courses. You may be well-versed on modern serial protocols but learning parallel-bus protocols of DDR DRAM will be valuable. You might have worked extensively with mainstream PC DRAMs and now you need to learn low-power LP DRAM designs. Any time your work requires you to design, develop, validate, verify, test, debug or support DRAM interfaces, you should seriously consider taking MindShare's classes.

You Will Learn:

- Where JEDEC expects DRAM to appear in a system
- How a DRAM cell is addressed by the controller
- Difference between Banks, Bank Groups and Ranks
- Why the DRAM controller is so complicated
- Activation, Precharge and Refresh
- DDR4 pin definitions
- DDR4 bank state diagram
- DDR4 timing waveforms
- Prefetch Width
- Types of DIMMs
- Fly-By Routing
- DDR5/LPDDR4/LPDDR5 pin definitions
- DDR5/LPDDR4/LPDDR5 bank state diagrams
- DDR5/LPDDR4/LPDDR5 timing waveforms
- DDR5 DIMM PMIC
- Intro to NVDIMM
- Newer forms of Refresh
- POD and LVSTL signaling
- Clock throttling and dynamic voltage changes
- On-Die Termination (ODT)
- JEDEC Initialization and Mode Registers
- Calibration and training, including
    - Vref training
    - Read and Write calibration
    - Write Leveling
- Sources of errors and JEDEC features for handling errors
- Test philosophy and JEDEC features to assist with testing

Course Length: 4 Days

Who Should Attend?

This course is hardware-centric and also describes initialization and training of DRAM devices and controllers. It is suitable for hardware engineers and software/firmware engineers will also benefit. The course is ideal for DRAM controller designers, chipset designers, system board-level design and validation engineers.

This course introduces current DRAM technologies, concentrating on DDR4 as a baseline to teach concepts that are common to all DRAMs. The course then continues to cover in detail all new features of DDR4, DDR5, LPDDR4, and LPDDR5.

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Course Contents:

- System Architecture
  - PC Platform Architecture
  - NUMA Architecture
  - SoC Architecture
- Back to the Future DRAM Intro
  - It's more similar than it is different
- DRAM Cell Architecture
  - Problems of Activation, Precharge and Refresh
- DRAM Device Architecture
  - SDRAM through DDR5
  - DDR4/DDR5 Bank Groups
  - LPDDR4, LPDDR5
  - LPDDR5 Bank Groups
- Packaging
  - Monolithic
  - Stacked Die
  - 3DS, Hybrid Memory Cube, High Bandwidth Memory (HBM)
  - Package-on-Package
  - Dual LPDDR4 Channels
- DRAM Controller Basics
  - Functional Blocks
  - Address Translation/Address Mapping Examples
- Device and Dual In-line Memory Module (DIMM) Pin Descriptions
  - DDR4
  - DIMM
- Introduction to DIMM Architecture
  - UDIMM
  - RDIMM
  - LRDIMM
  - Fly-by Routing
- Bank State Machines, Commands, Waveforms
  - DDR4
- Refresh
  - Auto Refresh
  - Self Refresh
  - Auto Self Refresh
- Device and DIMM Pin Descriptions
  - DDR5
  - DIMM
  - LPDDR4
  - LPDDR5
- DDR4 and DDR5 DIMM Architecture
  - UDIMM
  - RDIMM
  - LRDIMM
  - NVDIMM
  - PMIC
  - DDR4 On-DIMM Address Mirroring
  - DDR5 Mirroring

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- Bank State Machines, Commands, Waveforms
  - DDR5
  - LPDDR4
  - LPDDR5
- Newer Forms of Refresh
  - Per-Bank and Fine Granularity Refresh
  - Temperature Compensated Refresh
  - Self-Refresh Abort, Fast Exit
- Electrical Specifications
  - DDR4/DDR5 POD
  - LPDDR4/LPDDR5 LVSTL
  - IDD Specifications, Example
- Power Management
  - Power Down and Self Refresh
  - DDR4/DDR5 Max Power Saving Mode
  - LPDDR4/LPDDR5 Frequency Setpoints (FSP)
  - LPDDR5 Dynamic Voltage and Frequency Scaling
- Introduction to Signal Integrity Issues
  - Sources and Solutions
  - Derating and Margining
- On-Die Termination
  - Sync/Async ODT
  - DDR4/DDR5 Dynamic ODT
  - LPDDR4 Data Group ODT and Command Bus ODT
  - DDR4/DDR5 Park Mode
  - DDR5 Command Bus ODT
- Initialization, Calibration and Training
  - JEDEC Initialization
    - DDR4, DDR5 Mode Registers
    - DDR4, DDR5 Initialization
    - LPDDR4, LPDDR5 Mode Registers
    - LPDDR4, LPDDR5 Initialization
  - Calibration and Training
    - ZQ Calibration
    - Internal Vref Training
    - CA Command Bus Training
    - Read Calibration
      - Including Duty Cycle Adjustment
    - Write Calibration
      - Including DFE, FIFO, DQS Oscillator and Loopback
    - Write Leveling
- Errors and Error Handling
  - Sources of Errors
  - DIMM ECC
  - DDR5 On-Die ECC
  - DIMM Parity
  - DDR4 CA Parity
  - DDR4 Write CRC
  - DDR5 Read/Write CRC
  - LPDDR5 Link ECC
  - MR Readout via Multi-Purpose Register
  - Row Hammer and Target Row Refresh
  - Post Package Repair

- Testing
  - DRAM Functional Tests
  - Structural Test Example
  - Cell Test Example
  - DRAM Parametric (pin) Tests
  - DDR4 Connectivity Test Mode
  - DDR5 Loopback Mode
- Optional Topics
  - SMBus Overview, I3C
  - NVM Transaction Overview

Recommended Prerequisites:

Fundamental

A basic understanding of digital logic.

Course Material:

1. Students will be provided a softcopy of the presentation materials used in class.
2. Add-On DRAM (DDR5/LPDDR5) Architecture eLearning course (discounted pricing applies) which can be used after course completion for review or to cover topics not covered in class.