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www.mindshare.com

DRAM (DDRx/LPDDRx) Architecture Course Info

Let MindShare Bring "DRAM (DDRx/LPDDRx) Architecture" to Life for You

Ever since Intel introduced DRAM memory, it has evolved in size, density, speed and architecture. It has also evolved in power consumption, most notably with the Low-Power DDRs. DRAMs have evolved to DDR4 and LPDDR4. MindShare's DRAM Architecture course describes the development of computer memory systems and covers in-depth today's most advanced DRAM technology. The course ultimately focuses on ultra-dense, high-speed DDR3/DDR4/LPDDR3/LPDDR4 technology. Memory cell theory, operation and key device architecture differences from SDRAM through DDR4 as well as LPDDR1 through LPDDR4 are covered. The PC DIMM organization is covered, as well as bus implementations. Initialization of a memory channel is described. System design challenges, ranging from signal routing to error handling, are covered. Using waveform examples, state diagrams and truth tables, the commands and correct sequencing of operations are taught. DRAM controller design principles are also discussed.

You Will Learn:

- How a DRAM array is organized
- Organization of a variety of memory modules
- How to understand DRAM transaction waveforms so that you can debug a memory channel
- How to refresh a DRAM
- Electrical characteristics of DDRx and LPDDRx signals
- Elements of DRAM controller design
- Differences between DDR1 through DDR4 as well as LPDDR1 through LPDDR4
- DRAM power management
- Error handling

Course Length: 3 Days

Who Should Attend?

This course is hardware centric but does describe DRAM memory and DRAM controller initialization. It is suitable for hardware engineers, but software/firmware engineers will benefit. The course is ideal for DRAM controller designers, chipset designers, system board-level design and validation engineers.

Course Contents:

- System Architecture
  - PC Platform Architecture
  - NUMA Architecture
  - SoC Architecture
- Back to the Future DRAM Intro
  - It's more similar than it is different
- DRAM Cell Architecture
- DRAM Device Architecture
  - SDRAM thru DDR4
  - DDR4 Bank Groups
  - LPDDR3, LPDDR4, and WideIO
- DDRx/LPDDRx Feature Summary, Comparison, and Roadmap
  - DDR4 New Features
  - LPDDR4 New Features
- DRAM Controller Basics
  - Block Diagram
  - What is the address?

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- Packaging DDR3, DDR4, LPDDR3, LPDDR4, WideIO
  - Monolithic
  - Stacked Die
  - WideIO Stack
  - 3DS
  - Package-on-Package
  - Stacked Package
  - Dual LPDDR4 Channels
- DDR3 and DDR4 Module Architecture
  - UDIMM
  - RDIMM
  - LRDIMM
- Device and Module Pin Descriptions
  - DDR3, DDR4
  - DIMM
  - LPDDR3, LPDDR4
- Commands and Waveforms
  - DDR3, DDR4
  - LPDDR3, LPDDR4
- Refresh
  - Auto Refresh
  - Self Refresh
  - Auto Self Refresh
  - Fine Granularity Refresh
  - Self Refresh Abort
  - Fast Exit Self Refresh
  - Row Hammer and LPDDR4 Target Row Refresh
- Electrical Specifications
  - DDR3 SSTL
  - DDR4 POD
  - LPDDR3 HSUL
  - LPDDR4 LVSTL
  - IDD
- Power Management
  - Active and Precharge Power Down
  - LPDDR3 Deep Power Down, DDR4 Max Power Saving Mode
  - Self Refresh, Temperature Compensated
  - Clock Throttling
- Introduction to Signal Integrity Issues
- Signal Routing
  - Trace-length matching
  - DDR3/DDR4 Fly-by Routing
  - DDR3/DDR4 On-DIMM Address Mirroring
  - LPDDR4 Dual Channels
- On-Die Termination
  - Sync/Async ODT
  - DDR3/DDR4 Dynamic ODT
  - LPDDR3/4 Data Group ODT, LPDDR4 Command Bus ODT
  - DDR4 Park Mode
- Initialization, Calibration, and Training
  - JEDEC Initialization
    - DDR3, DDR4, LPDDR3, LPDDR4 Mode Registers
    - DDR3, DDR4 Initialization

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        - LPDDR3, LPDDR4 Initialization
    - Calibration and Training
        - ZQ Calibration
        - Data Training / DQ Cal. / Read Cal.
        - Write Leveling
        - LPDDR3/4 CA Training / Command Bus Training
        - DDR4 Geardown Mode
        - DDR4/LPDDR4 Internal Vref Training
- Errors and Error Handling
    - Sources of Errors
    - Hard Errors and Soft Errors
    - Internal Errors and External Errors
    - DDR4/LPDDR4 Post Package Repair
    - DIMM ECC
    - DIMM Parity
    - DDR4 CA Parity
    - DDR4 Write CRC
    - Multi-Purpose Register
    - MRS Readout
- Introduction to Testing
    - DRAM Functional Tests
    - DRAM Parametric (pin) Tests
    - Controller Functional Tests
    - Controller Parametric Tests
    - DDR4 Connectivity Test Mode
- Optional Topics
    - SMBus Overview
    - Other Types and Form Factors for DRAM
    - GDDR5 Overview

Recommended Prerequisites:

A basic understanding of digital logic.

Course Material:

Students will be provided with soft-copy of presentation material used in class