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DRAM (DDRx) Architecture Course Info

Let MindShare Bring "DRAM (DDRx) Architecture" to Life for You

Ever since Intel introduced DRAM memory, it has evolved in size, density, speed and architecture, to the current DDR4 standard. MindShare's DRAM (DDRx) Architecture course describes the development of computer memory systems and covers in-depth DRAM technology. The course focuses DDR3 and DDR4 technology. Memory cell theory, operation and key chip architecture differences from SDRAM through DDR4 are covered. The PC DIMM organization is covered, as well as bus implementations. Initialization of a memory channel is described. System design challenges, ranging from signal routing to error handling, are covered. Using waveform examples, state diagrams and truth tables, the commands and correct sequencing of operations are taught. DRAM controller design principles are discussed.

You Will Learn:

- How a DRAM array is organized
- Organization of a variety of memory modules
- How to understand DRAM transaction waveforms so that you can debug a memory channel
- How to refresh a DRAM
- How to initialize and train a DRAM channel
- Electrical characteristics of DDR3 (SSTL) and DDR4 (POD)
- Elements of DRAM controller design
- Differences between DDR1 through DDR4
- DRAM power management issues
- Error handling

Course Length: 2 Days

Who Should Attend?

This course is hardware centric but does describe DRAM memory and DRAM controller initialization. It is suitable for hardware engineers, but software/firmware engineers will benefit. The course is ideal for DRAM controller designers, chipset designers, system board-level design and validation engineers.

Course Contents:

- System Architecture
  - PC Platform Architecture
  - NUMA Architecture
- Back to the Future DRAM Intro
  - It's more similar than it is different
- DRAM Cell Architecture
- DRAM Device Architecture
  - SDRAM thru DDR4
  - DDR4 Bank Groups
- DRAM Controller Basics
  - Block Diagram
  - What is the address?
- Packaging
  - Monolithic
  - Stacked Die
  - 3DS Hypercube
  - Stacked Package
- PC DDRx/LPDDRx Feature Summary, Comparison, and Roadmap
  - DDR4 New Features
- DDR3 and DDR4 Module Architecture

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  - UDIMM
  - RDIMM
  - LRDIMM
- Device and Module Pin Descriptions
  - DDR3, DDR4
  - DIMM
- Commands and Waveforms
  - DDR3, DDR4
- Refresh
  - Auto Refresh
  - Self Refresh
  - Auto Self Refresh
  - Fine Granularity Refresh
  - Self Refresh Abort
  - Fast Exit Self Refresh
- Electrical Specifications
  - DDR3 SSTL
  - DDR4 POD
  - IDD
- Power Management
  - Active and Precharge Power Down
  - DDR4 Max Power Saving Mode
  - Self Refresh, Temperature Compensated
  - Low-power Auto Self Refresh
  - Clock Throttling
- Introduction to Signal Integrity Issues
- Signal Routing
  - Trace-length matching
  - DDR3/DDR4 Fly-by Routing
- On-Die Termination
  - DDR3 and DDR4 Dynamic ODT
  - Sync/Async ODT
  - DDR4 Park Mode
- Initialization, Calibration, and Training
  - JEDEC Initialization
    - Mode Registers
    - Initialization
  - Calibration and Training
    - ZQ Calibration
    - Data Training / DQ Cal. / Read Cal.
    - Write Leveling
    - DDR4 Geardown Mode
    - DDR4 Internal Vref for DQ
- Errors and Error Handling
  - DDR4 CA Parity
  - DDR4 Write CRC
- Testing
  - DDR4 Connectivity Test Mode

Recommended Prerequisites:

A basic understanding of digital logic.

Course Material:

Students will be provided with soft-copy of the presentation material used in class