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Fundamentals of DRAM (DDRx/LPDDRx) Architecture Course Info

Let MindShare Bring "DRAM (DDRx/LPDDRx) Architecture" to Life for You

Whether you are new to DRAM or an industry veteran seeking the latest and greatest standards, you will learn more than you expect from MindShare's DRAM courses. You may be well-versed on modern serial protocols but learning parallel-bus protocols of DDR DRAM will be valuable. You might have worked extensively with mainstream PC DRAMs and now you need to learn low-power LP DRAM designs. Any time your work requires you to design, develop, validate, verify, test, debug or support DRAM interfaces, you should seriously consider taking MindShare's classes.

You Will Learn:

- Where JEDEC expects DRAM to appear in a system
- How a DRAM cell is addressed by the controller
- Difference between Banks, Bank Groups and Ranks
- Why the DRAM controller is so complicated
- Activation, Precharge and Refresh
- DDR4/DDR5/LPDDR4/LPDDR5 device architecture overview
- Prefetch Width
- Types of DIMMs
- Fly-By Routing

Course Length: 1 Day

Who Should Attend?

This course is hardware-centric and also describes initialization and training of DRAM devices and controllers. It is suitable for hardware engineers and software/firmware engineers will also benefit. The course is ideal for DRAM controller designers, chipset designers, system board-level design and validation engineers.

Fundamentals of DRAM introduces current DRAM technologies, concentrating on DDR4 to teach concepts that are common to all DRAMs.

Course Contents:

- System Architecture
  - PC Platform Architecture
  - NUMA Architecture
  - SoC Architecture
- Back to the Future DRAM Intro
  - It's more similar than it is different
- DRAM Cell Architecture
  - Problems of Activation, Precharge and Refresh
- DRAM Device Architecture
  - SDRAM through DDR5
  - DDR4/DDR5 Bank Groups
  - LPDDR4, LPDDR5
  - LPDDR5 Bank Groups
- Packaging
  - Monolithic

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  - Stacked Die
  - 3DS, Hybrid Memory Cube, High Bandwidth Memory (HBM)
  - Package-on-Package
  - Dual LPDDR4 Channels
- DRAM Controller Basics
  - Functional Blocks
  - Address Translation/Address Mapping Examples
- Device and Dual In-line Memory Module (DIMM) Pin Descriptions
  - DDR4
  - DIMM
- Introduction to DIMM Architecture
  - UDIMM
  - RDIMM
  - LRDIMM
  - Fly-by Routing
- Bank State Machines, Commands, Waveforms
  - DDR4
- Refresh
  - Auto Refresh
  - Self Refresh
  - Auto Self Refresh

Recommended Prerequisites:

A basic understanding of digital logic.

Course Material:

Students will be provided a softcopy of the presentation materials used in class.