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High Bandwidth Memory (HBM1/HBM2/HBM2E/HBM3/HBM3E) Architecture Training

Let MindShare Bring "High Bandwidth Memory Architecture" to Life for You

High Bandwidth Memory (HBM) is a form of DRAM used on the most capable HPC and SoC platforms. HBM is an evolution of WideIO and WideIO2 with some concepts borrowed from Graphics DRAM. HBM provides the maximum possible bandwidth of any DRAM technology, largely by implementing several very wide channels. All DRAM (PC DRAM, LP DRAM, Graphics DRAM, HBM) are very similar to one another, but there are significant differences in HBM that this course covers in detail.

You Will Learn:

- DRAM architecture fundamentals if you book a 3-Day class
- Where JEDEC expects HBM to be placed in a system
- Organization and operation of HBM devices
- Electrical characteristics of HBM and why HBM lacks many SI tools found in other technologies
- Differences between WideIO, WideIO2, HBM1, HBM2, HBM2E, HBM3 and HBM3E
- Calibration and training of HBM channels
- HBM power management
- HBM error handling
- Overview of IEEE 1500

Course Length: 4 Days (or 3 Days if you have DRAM Fundamentals background)

Who Should Attend?

This course is hardware centric but does describe DRAM memory and DRAM controller initialization. It is suitable for hardware engineers, but software/firmware engineers will benefit. The course is ideal for DRAM controller designers, chipset designers, system board-level design and validation engineers.

Course Contents:

DRAM Fundamentals (1 Day can be skipped with DRAM fundamentals prerequisite knowledge)

- System Architecture and Intro to DRAM
- DRAM Device Architecture
- Packaging and HBM
- DRAM Controller Basics and Addresses
- DDR4 Device and Pin Descriptions
- Signal Routing
- DDR4 - Bank State Machines, Commands and Waveforms
- Refresh

HBM Topics (3 Days)

- System Architecture and Packaging
  - Example Platforms
- Channel Architecture, Device Organization and Device Architecture
  - Features and Architectures of Previous Technologies (PC and LP DRAMs)
  - HBM Channels and Pseudo channels
- Signal Descriptions
  - Channel Signals
  - Global Signals

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- Bank State Machines, Commands and Waveforms
  - Simultaneous Row and Column Commands
  - Use of WDQS and RDQS
- Refresh
  - Auto Refresh
  - Self Refresh
  - Single-bank (Per-bank) Refresh
  - Row Hammer, Target Row Refresh and Refresh Management
- Electrical Specifications
  - Why so many traditional SI tools (ODT, ZQ cal, Write Leveling, etc.) are not present
  - IDD Specification
- Power Management
  - Power Down
  - Clock Throttling
- Initialization, Calibration, and Training
  - JEDEC Initialization
    - Mode Registers
    - Initialization Steps
  - Calibration and Training
    - Vref Training
    - Loopback LFSR MISR Training
      - Command Bus (AWORD) Training
      - Data Group (DWORD) Training
    - Duty Cycle Adjustment (DCA) and Duty Cycle Monitoring (DCM)
    - WDQS Interval Oscillator
- Errors and Error Handling
  - Temperature
  - Address Parity
  - Data Parity
  - Channel Remapping
  - On-Die ECC
  - Post Package Repair
    - Self-Repair
    - Hard and Soft Repair
- Overview of IEEE 1500

Recommended Prerequisites:

Completion of MindShare's Fundamentals of DRAM course or equivalent industry experience for a 3 Day class, otherwise for 4 Day class, digital design and computer architecture background.

Course Material:

- Soft copy of presentation material used in class
- HBM Architecture eLearning (when available)