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Hands-On Intel Haswell/Broadwell CPU

Training

Let MindShare Bring "Intel Haswell/Broadwell CPUs" to Life For You

Each generation of core architecture Intel64 and IA-32 Instruction Set Architecture (ISA) platform brings new capabilities while maintaining backward compatibility with earlier x86 family members. Building on features introduced in the earlier processors, the latest 22nm Haswell and 14nm Broadwell CPUs bring a new microarchitecture and significant enhancements in areas including instruction throughput, power conservation, and integrated graphics. In addition, system-on-a-chip (SOC) packaging options, combining the CPU and platform controller hub (PCH) onto a single multi-chip module, are also offered.

The primary focus of this course is on the architecture and initialization of the CPU itself. Topics include CPU operational modes, instruction pipeline, execution units, registers, cache architecture, local APICs, virtualization support, etc. Integrated CPU system agent and graphics logic is also described. To promote a more complete level of understanding, an overview of platform chipset support and SOC implementations built around Haswell/Broadwell is provided. Note that other MindShare live and eLearning courses offer more comprehensive coverage of some of the topics introduced in this course, including: including x86 software, DRAM technology, PCIe, USB 3.0, SATA, Virtualization, etc.

Many internal CPU/SOC features as well as their bridges/controllers for external bus interfaces are managed as PCI functions—each with some combination of IO, MMIO, and PCI Configuration Space registers which must be initialized by BIOS or other software. Hands-on lab exercises integrated into this course enable students to examine the decoded contents of PCI, IO, and MMIO registers, CPU model-specific registers (MSRs), as well as main memory data structures using MindShare's Arbor software tool. The exercises allow students to determine both CPU/SOC capabilities and the manner in which they have actually been configured. In addition to previously captured system scans distributed with Arbor software, students may use Arbor to scan their local systems, read/modify registers, and save scan results for later sharing and off-line review.

You Will Learn:

- Haswell/Broadwell CPU and Platform Variants
- Caches and coherency protocol
- Instruction Pipeline and Execution Units
- Registers
- CPU Operational Modes
- Processor Graphics
- Power and Thermal management
- Interrupt Handling
- Machine Check Architecture (MCA)
- CPU initialization
- Performance Monitoring Capabilities
- External CPU Interfaces
- Processor Virtualization Support

Course Length: 4 Days

Course Outline:

- Intel Core Architecture CPU Background
  - Intel 64 and IA-32 CPU lineage: 80386 to Haswell/Broadwell
- Haswell/Broadwell CPU and Platform Examples
  - Intel Core i3/i5/i7 Mobile (SOC)
  - Intel Xeon E5 Workstation CPU
  - Intel Xeon E7 Server CPU
  - **Class exercise:** *Intel ARK CPU & SOC feature comparison*

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- Platform Addressing
  - Traffic types
    - Programmed IO (PIO)
    - Direct memory access (DMA)
    - Peer-to-Peer
  - System Memory Addresses
    - DRAM Main Memory
    - Memory Mapped IO (MMIO)
    - Addressing Memory Space using CPU *MOV* Instructions
  - System IO addresses
    - Legacy IO
    - Limitations of IO space accesses
    - Accessing IO space CPU *IN and OUT* Instructions
  - PCI Configuration Space
    - Motivation
    - PCI topology rules and Bus/Device/Function (BDF) numbers
    - CPU access of PCI space: two methods
    - Legacy method: IO space access
    - Newer method: MMIO space access
    - PCI Configuration Space structures within the CPU/SOC
  - **Arbor lab:** *CPU Host Bridge PCI BARs and system memory map management*
- Processor Internal Architecture
  - Some x86 terminology
  - Processor role: Fetch/Decode/Execute
    - X86 code basics
    - Motivation for CISC to uOp decoding
    - Superscalar, parallel execution
  - CPU Resources: Dedicated vs. Shared
  - Instruction Pipeline
    - Instruction Fetch Unit (IFU)
    - Instruction Length Decoder/Predecode (ILD)
    - Branch Prediction Unit (BPU)
    - Instruction Queue (IQ) and Macro-fusion
    - Decoders/Micro-Fusion
    - uCode ROM
    - uOp Cache
    - Instruction Decoder Queue (IDQ)
    - Allocation/Rename/Retire (RAT)
    - Physical Register File (PRFs)
    - Reorder Buffer (ROB)
    - Load and Store Buffers
  - Reservation Station (RS) And Execution Units
    - Overview of uOP Dispatch And Execution
    - Role Of The Eight Reservation Station Ports
    - Execution Unit Clusters
    - Disambiguation
  - Register Set
    - Control Registers
    - General Purpose Registers (GPRs)
    - Debug Registers
    - Floating Point Registers
    - SIMD Registers
    - Model Specific Registers (MSRs)
    - Segmentation Registers
  - Implications of HyperThreading
    - Replicated, Partitioned, Competitively shared resources
    - Performance
  - **Arbor lab:** *Examining CPU Architectural Features*

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- CPU Address Generation Details
  - CPU operational mode affects addressing
  - Introduction to Physical Address Translation
  - Segmentation and Paging
    - Real Mode Segmentation
    - Protected Mode Segmentation
  - Demand Mode Paging
    - Basic 4K Paging
    - PAE, PSE Engancements
    - Translation Look-Aside Buffer (TLB) Architecture
  - Impact of IA32e 64-bit Extensions on Physical Address Translation
- L1 and L2 Caches
  - Five Memory Types
  - Cache Policy Setup: MTRRs
  - Cache Policy Setup: Paging Structures
  - L1, L2, L3 Cache Hardware Architecture
  - CPU Rules Of Conduct: UC/WC And WB/WT/WP Regions
  - Miscellaneous Cache Topics:
  - PAT Feature
  - Software Prefetch Instruction
  - Non-temporal Data
  - Direct Data IO (DDIO)/Direct Cache Access (DCA)
- Processor Graphics And Display
  - Haswell/Broadwell Graphics Feature Summary: GT1, GT2, GT3
  - 2D and 3D Graphics uArchitecture Elements
  - Display Support

- Platform Interrupt Handling
  - Background
  - APIC/IOAPIC and Local APICs
  - Message Signaled Interrupt (MSI/MSI-X) Basics
  - CPU Interrupt Servicing
- CPU Management Topics
  - Power Management
  - Thermal Management
  - **Arbor Lab:** *CPU Power/Thermal Management (combined lab)*
  - System Management Mode (SMM)
  - Error Handling and Machine Check Architecture (MCA)
  - Microcode Update
- Overview of Key External CPU Interfaces
  - Main Memory DRAM
  - Direct Media Interconnect (DMI)
  - QuickPath Interconnect (QPI)
  - PCI Express (PCIe)
- Other Topics
  - Processor Virtualization Support
  - Performance Monitoring

Recommended Prerequisites: a basic understanding of computer architecture is very helpful

Course materials:

1) Course presentation PDF
2) MindShare's "x86 Instruction Set Architecture" eBook by Tom Shanley
3) MindShare Arbor Software learning/test/debug tool