Hands-On USB 3.1 with xHCI

Training

Let MindShare Bring “Hands-On USB 3.1 with xHCI” to Life for You

The Universal Serial Bus (USB) is the most widely used IO interface in the world. Each generation through USB 2.0 is backward compatible and, depending on the capabilities of the attached devices, operates at one of the three data rates over the USB 2.0 half-duplex signal interface. The active rate is referred to as Low, Full, or High Speed. USB 3.0 and USB 3.1 added an additional set of signals to cables and connectors to support two more data rates, SuperSpeed and SuperSpeedPlus. Because USB 2.0 and SuperSpeed are physically separate in cables/connectors and even hubs, USB 3.1 refers to devices operating at Low, Full, or High Speed as being part of the USB 2.0 topology; devices operating at SuperSpeed or SuperSpeedPlus are part of the Enhanced SuperSpeed topology. It is important to note that in addition to the faster data rates, the Enhanced SuperSpeed topology includes a number of other major optimizations including directed (unicast) packets, better flow control, device asynchronous messages, as well as link level error handling and power management.

All generations of USB rely on platform USB host controllers to manage devices attached to each bus instance. USB 1.1 and USB 2.0 employed UHCI/OHCI and EHCI compliant host controllers to handle Low, Full, and High Speed devices. The advanced capabilities of USB 3.1 Enhanced SuperSpeed require a new generation of host controller. This course covers the major features of one of the most important classes of USB 3.x host controllers, those based on Intel’s eXtensible Host Controller Interface (xHCI). A single xHCI host controller can manage both USB 2.0 and Enhanced SuperSpeed topologies as well as attached devices of any USB speed. xHCI topics also include its improvements to earlier host controller models in the areas of hardware transaction scheduling, doorbell-based work notification, and many others.

Hands-on lab exercises integrated into this course enable students to examine the USB descriptors of mass storage, hub, and other standard class devices. In addition, decoded contents of xHCI host controller registers and main memory data structures required to manage attached devices are evaluated using MindShare’s Arbor software tool. The exercises allow students to determine both device and host controller capabilities, as well as the manner in which they are actually programmed in a real-world system. Several saved Arbor system scans are distributed with Arbor software and students may use Arbor to scan their local systems, read/modify registers, and save scan results for later sharing and off-line review.

Who Should Attend?

This five-day course is designed for hardware, software, validation engineers and anyone else needing both the protocol view USB 3.1 as well as insight into how these systems are commonly initialized and managed. Features and limitations of each generation of USB are described as is the role of xHCI compliant host controllers in managing USB devices and hubs of all types.

Course Length: 5 Days

Course Outline:

Part 1: Course Scope, Background, and Overview
• USB 3.1 System Topology, The Big Picture
  o A USB 2.0 Elements
  o USB 2.0 Elements
  o Enhanced SuperSpeed Elements
• USB 2.0 Background
  o Original USB Motivations
  o USB 2.0 Topologies
  o Device Requests
  o USB 2.0 Packet Protocol
  o USB 2.0 Transaction Generation and Scheduling
  o USB 2.0 Device VBus Power
Class exercise: Evaluating a USB 2.0 Topology

USB 3.0 Background
- USB 3.0 Composite Cable
- Layered Protocol Model for USB 3.0 SuperSpeed Interfaces
- USB 3.0 Hubs
- Simple SuperSpeed Transaction Examples
- Link Level Error Handling
- Link Level Header Packet Flow Control (Credit Based)
- New Device Requests and SuperSpeed Descriptors
- SuperSpeed Link Power Management Enhancements

Class exercise: Evaluating a USB 3.0 Topology

Features Introduced in USB 3.1
- Enhanced SuperSpeed Host Controller Logic
- Protocol Layer Changes
- Link Layer Changes
- Physical Layer Changes
- USB 3.1 Hubs

Part 2: USB 3.0 Protocol Details

SuperSpeed End-to-End Protocol
- Overview of End-to-End Packets
- Control Protocol
  - Two-Stage Control Transfers
  - Three-Stage Control Transfers
- Bulk Protocol
  - Bulk IN and Bulk Out Transfers
  - Flow Control and Error Handling
  - Data Bursting and Streaming Options
  - Examples: UAS and UASP Commands

Class exercise: Protocol Analyzer View of SuperSpeed data transactions
- Interrupt Protocol
  - Interrupt IN and Interrupt OUT Transfers
  - Flow Control and Error handling
  - Data Bursting Option
- Isochronous Protocol
  - Introduction and Motivation
  - Bus Intervals and Isochronous Service Scheduling
  - Isochronous IN and Isochronous OUT Transfers
  - Multiple Burst Option
  - Isochronous Timestamp Packet (ITP)

SuperSpeed Port-to-Port Protocol
- Link Training and Status State machine (LTSSM)
- Link Commands
  - Packet Acknowledgement Link Commands
  - Flow Control Link Commands
  - Power Management Link Commands
  - Link Up (LUP) and Link Down (LDN) Link Commands
- Header Packet Processing
  - Link Sequence Number Assignment
  - CRC-5 and CRC-16 Generation and Checking
  - Header Packet Buffers
- Header Packet Flow Control
  - Transmitter and Receiver Link Layer Flow Control logic
  - Usage model
- Link Errors and Packet Acknowledgement
  - Error types
  - Transmitter and Receiver Link Layer Packet Acknowledgement logic
  - Header Packet Acknowledgement and Retry mechanism

SuperSpeed Chip-to-Chip Protocol
- Physical Layer (PHY) Logical Functions
  - Transmitter Physical Layer Logic
  - Receiver Physical Layer Logic
- SuperSpeed Reset Events
- PowerOn Reset
- Warm Reset and Hot Reset

- Link Training
  - The Link Training Sequence
  - Initial Sequence Number and Flow Control Credit Advertisement
  - Port Configuration
- **Class exercise:** Protocol Analyzer View of SuperSpeed Link Training
- Link Recovery and Retraining

- USB 3.0 Hubs
  - Packet Forwarding
  - Hub Error Detection and Handling
  - Hub Link Power Management Responsibilities
  - Cable Power and Distribution
  - Reset Propagation

- Device Configuration
  - Standard Requests
  - Device Detection and Reporting
  - The Device Configuration Process
  - Additional Considerations for USB 3.1 Devices
- **Class exercise:** Protocol Analyzer View of Device Configuration

- Hub Configuration

- SuperSpeed Power Management
  - USB 3.0 vs. USB 3.1 Features
  - Basic Principles
  - Link Power Management
  - Software Role in Link Power Management
  - Suspend And Resume
  - Platform Power Management Issues

- SuperSpeed Signaling Requirements
  - SuperSpeed Transmitter Requirements
  - SuperSpeed Receiver Requirements

- SuperSpeed Compliance Testing
  - Scope
  - USB Command Verifier Compliance
  - Link Layer Compliance
  - Electrical Compliance Testing
- **SuperSpeed Receiver Loopback and Bit Error Rate Test (BERT)**
  - Loopback Configuration
  - Required and Optional Bit Error Rate Test (BERT) Capabilities

Part 3: USB 3.1 Protocol Changes

- Protocol Layer Changes for SuperSpeedPlus (Gen 2)
  - Type 1 and Type 2 packet priority
  - Transaction Packets
    - Transaction Packet Header (TPH) fields
    - New Device Notifications
  - Data Packets
    - Data Packet Header (DPH) fields
    - Data Packet Payload (DPP) fields
    - SuperSpeedPlus burst transaction time limits
  - Isochronous Timestamp Packet fields
  - Link Management Packets (LMPs)
  - Transaction ordering and reordering
    - Transaction Packets vs. Data Packets
    - Periodic vs. asynchronous endpoint packets
    - Type 1 vs. Type 2 packets
    - Ordering packets targeting same/different endpoints
  - **Precision Time Measurement (PTM)**
    - Link Delay Measurement (LDM)
    - Hub Delay Measurement (HDM)
Device Framework changes
  • Requests
  • Descriptors

Link Layer Changes for SuperSpeedPlus
  • Framing ordered sets
  • New deferred and non-deferred Data Packet Header (DPH)
  • Logical Idle
  • Link HP Buffers and flow control
    ▪ Two sets of Tx/Rx HP Buffers
    ▪ Two types of flow control credit link commands
  • Link error handling
    ▪ New link error types
    ▪ Optional Soft Error Count
  • LTSSM and link training changes

Physical Layer Changes for SuperSpeedPlus
  • New symbols/ordered sets
  • Low Frequency Periodic Signaling (LFPS) variants
  • Tx/Rx PHY Logical section
    ▪ Scrambling/Descrambling
    ▪ 128b/132b Encoding/Decoding
    ▪ Rx Elastic Buffer
  • Tx/Rx PHY Electrical section
    ▪ Signaling requirements
    ▪ Tx/Rx equalization

USB 3.1 Hubs
  • Store and forward architecture
  • Buffering
  • Hub arbitration of upstream and downstream packets
  • SuperSpeed and SuperSpeedPlus rate matching

Part 4: eXtensible Host Controller Interface (xHCI) for USB
  • xHCI Role and USB 3.x Software-Hardware Layers
  • Host Controller Hardware Options and Topology Examples
  • xHCI Operational Model
    ▪ Host Controller Initialization
      ▪ PCI Configuration Registers
      ▪ Memory Mapped IO Registers
      ▪ Arbor Exercise: xHCI Host Controller Register Setup
    ▪ Device Attachment/Removal and Slot Management
      ▪ Detecting and Reporting
      ▪ Resource Allocation
    ▪ Using the Primary xHCI Memory Data Structures
      ▪ Device Context
      ▪ Transfer Rings And TRBs
      ▪ Arbor Exercise: Evaluating a Device Context, Transfer Ring, and TRBs
      ▪ Doorbell Request Scheme
      ▪ Command Ring
      ▪ Event Rings and Interrupters
      ▪ Arbor Exercise: Event Ring and Interrupts
    ▪ Hardware-based Transaction Scheduling
      ▪ Periodic Endpoint Scheduling
      ▪ Non-periodic (Asynchronous) Endpoint Scheduling
  • Other xHCI Features and Capabilities

Recommended Prerequisites: Background in USB 2.0 protocol is helpful.

Course materials:
Students will be provided with:
1. An electronic (PDF) version of the presentation used in class
2. MindShare’s USB 3.0 Technology eBook by Don Anderson and Jay Trodden
3. MindShare Arbor Software test/debug tool