High-Speed Design

Let MindShare Bring “High-Speed Design” to Life for You
The speed of today’s logic devices mandates that the interconnect on PCBs must meet the high switching rise/fall times of these devices. Switching edges are in the 200ps to 300ps range and some devices have edges that reach 17ps. This results in high-speed design problems such as:

- A lack of control over impedance and reflections
- Crosstalk and bypassing failures
- Time delays, false triggering and reflections
- Failure to meet EMI and FCC requirements

It is the edge rate, more than frequency, which exacerbates high-speed design challenges. Even if your design is of moderate frequency, the edge rates can cause your design to exhibit high-speed effects.

You Will Learn:

- How to cost effectively design and layout a high-speed PCB without sacrificing signal integrity
- How to comply with Signal Integrity (SI) & EMI standards
- Cookbook design rules that ensure your PCB will function properly in the prototype stage

Course Length: 3 Days

Who Should Attend?

- Digital logic engineers and system architects
- EMC specialists
- Technicians
- PCB layout professionals
- IC designers
- Applications Engineers
- Engineering and project Managers

Course Contents:

- Fundamentals
  - Frequency, Time and Distance
  - Lumped Versus Distributed Systems
  - Four Kinds of Reactance
  - Ordinary and Mutual Capacitance & Inductance
  - EM Fields
  - Geometry, C, L, & Zo, interrelationships
  - C & L Resonance
- High-Speed Properties of Logic Gates
  - Quiescent vs. Active Dissipation
  - Driving Capacitive Loads
  - Input Power and External Power
  - TTL, CMOS, SiGe, In Pn, ECL, & GaAs; Output Power, Speed and engineering disciplines, Dv, di effects and Voltage Margins
ICs: Cu vs Al, what are the issues?
- Low K Di-electrics
- Intersymbol Interference (ISI), eye diagrams and jitter
- Shoot Through Current (SSO) and how to minimize it
- Ground Bounce, Lead Inductance, Simultaneous Switching Noise (SSN)
- Electronic Packages: QFPs, PGAs, SOIC, PLCC, BGA, COB, TAB, FC, CSP and their relationship to SI
- Lead Capacitance and Thermal Considerations

Measurement Techniques
- Rise Time and Bandwidth of Oscilloscopes and probes
- Self-inductance and Spurious Signal Pickup of a Probe Ground Loop
- How Probes Load Down a Circuit
- Special Probing Fixtures
- Avoiding Pickup from Probe Shield Currents
- Viewing a Serial Data Transmission System, the eye pattern closure: ISI, Skin effect and tan loss.
- PLL and DLLs
- Communications - SONET, SERDES, OC 192/768, Fiber
- Slowing Down the System Clock
- Observing Crosstalk
- Measuring Operating Margins
- Observing Metastable States in Flip-Flops

Transmission Lines
- The quality factor, Q, and why lumped circuits can ring and cause EMI.
- Infinite Uniform Transmission Line
- Effects of Source and Load Impedance
- Special Transmission Line Cases
- Determining Line Impedance & Propagation Delay using TDR and VNA
- Skin/proximity effect & Dielectric Loss
- The Capacitive Load - Zo and propagation delay
- Matching Zo with trace alterations (neckdowns) - minimizing the C load
- 90°, 45° bends - are they concerns?
- Even/odd, differential/common modes are their effects on LVDS.

Terminations
- End/Source/Middle Terminators
- AC Biasing for End Terminators, where should it be used and how to choose the capacitor
- Hairball networks, bifurcated lines and capacitive stubs
- Terminating differentials - Eliminating common mode and minimizing power
- What causes differentials unbalance?
- Diode and active terminators, Resistor Selection and Crosstalk in Terminators

Vias
- Mechanical Properties of Vias
- Capacitance & Inductance of Vias
- Return Current and Its Relation to Vias
- Through Hole, Blind, Buried, Micro Vias
- Intelligent Vias and autorouters
- Via discontinuity and via resonance concerns

Ground Planes and Layer Stacking
- High-Speed Current Follows the Path of Least Inductance
- Crosstalk in Solid and Slotted Ground Planes
• Inductive/capacitive ratios for micro strips, striplines, and asymmetric, dual, and edge LVDS
• Guard Traces - Do they stop crosstalk, can they resonate?
• Near-End and Far-End Crosstalk
• Separating analog from ECL/PECL and TTL/CMOS the concept of moats/floats/drawbridge
• Split planes - CMOS/TTL, PECL and analog using the same bias voltages
• How to Stack Printed Circuit Board Layers (e.g. 4, 6, and 10 layer) for Zo and crosstalk control, Cu fills on signal layers, minimizing warpage
• Interplane Capacitance - How thin, what material and stackup placement
• SIR vs. frequency, software for performing crosstalk and ground bounce tests

• Power Systems
  • Providing a stable Voltage Reference - Cu planes
  • Distributing Uniform Voltage - Sense lines, bulk C and interplane C
  • Choosing a Bypass Capacitor - Electrolytic/tantalum and ceramic
  • Power plane resonance - serial and parallel, how to minimize both
  • Designing a .1 ohm bypass system up to Fknee
  • Designing for constant ESR
  • IC die capacitance, discrete C in the IC package
  • Why the 0201 - Both for better bypassing and EMI control
  • Minimizing L-Capacitor layouts for SOICs, PLCCs, and various configurations of BGAs

• Connectors & Cables
  • Mutual and Series Inductance - How Connectors Create Crosstalk and EMI
  • Using Connectors on a Multidrop Bus (Z mismatch reflection) and how to match Zc to Zo
  • Measuring Coupling in a Connector
  • Continuity of Gnd Underneath a Connector
  • Special Connectors for High-Speed requirements - Crosstalk and matching Zo
  • Differential Signaling Through a Connector

• Buses
  • Multidrop systems: Drivers, Transceivers, PCI, BTL, GTL & RAMBUS
  • How they function, Clock rates, typical failures
  • ISI - Minimize the effect with Equalization and Preemphasis
  • LVDS: types, unbalance, noise, layout & making them function
  • Methods to speed up busses - Distributive driving and load capacitance matching

• Clock Distribution
  • Timing Margin and Clock Skew
  • Using Low-Impedance Drivers and Clock Distribution Lines
  • Source Term. of Multiple Clock Lines
  • Controlling Crosstalk on Clock Lines
  • Delay Adjustments - Serpentine traces/DACs and varisters for dynamic delay
  • Differential Distribution
  • Controlling Clock Signal Duty Cycle using the integrator
  • Source synchronous clocking, DDR & RDRAM

Recommended Prerequisites:
Basic knowledge of ICs, high-speed designs and PCB layouts. No advanced math is required though attendees will find it helpful to bring a scientific calculator to the course.

Course Material:
Are your company’s technical training needs being addressed in the most effective manner?

MindShare has over 25 years experience in conducting technical training on cutting-edge technologies. We understand the challenges companies have when searching for quality, effective training which reduces the students’ time away from work and provides cost-effective alternatives. MindShare offers many flexible solutions to meet those needs. Our courses are taught by highly-skilled, enthusiastic, knowledgeable and experienced instructors. We bring life to knowledge through a wide variety of learning methods and delivery options.

training that fits your needs

MindShare recognizes and addresses your company’s technical training issues with:

• Scalable cost training
• Just-in-time training
• Training in a classroom, at your cubicle or home office

• Customizable training options
• Overview and advanced topic courses

• Reducing time away from work
• Training delivered effectively globally
• Concurrently delivered multiple-site training

MindShare training courses expand your technical skillset

- PCI Express 2.0®
- Intel Core 2 Processor Architecture
- AMD Opteron Processor Architecture
- Intel 64 and IA-32 Software Architecture
- Intel PC and Chipset Architecture
- PC Virtualization
- USB 2.0
- Wireless USB
- Serial ATA (SATA)

- Serial Attached SCSI (SAS)
- DDR2/DDR3 DRAM Technology
- PC BIOS Firmware
- High-Speed Design
- Windows Internals and Drivers
- Linux Fundamentals

... and many more.

All courses can be customized to meet your group’s needs. Detailed course outlines can be found at www.mindshare.com

*PCI Express ® is a registered trademark of the PCISIG.
Engage MindShare

Have knowledge that you want to bring to life? MindShare will work with you to “Bring Your Knowledge to Life.” Engage us to transform your knowledge and design courses that can be delivered in classroom or virtual classroom settings, create online eLearning modules, or publish a book that you author.

We are proud to be the preferred training provider at an extensive list of clients that include:

ADAPTEC • AMD • AGILENT TECHNOLOGIES • APPLE • BROADCOM • CADENCE • CRAY • CISCO • DELL • FREESCALE
GENERAL DYNAMICS • HP • IBM • KODAK • LSI LOGIC • MOTOROLA • MICROSOFT • NASA • NATIONAL SEMICONDUCTOR
NETAPP • NOKIA • NVIDIA • PLX TECHNOLOGY • QLOGIC • SIEMENS • SUN MICROSYSTEMS • SYNOPSYS • TI • UNISYS