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High-Speed Design and EMI/EMC for Mobile Platforms

Training

Let MindShare Bring "High-Speed Design and EMI/EMC for Mobile Platforms" to Life For You

It is predicted that high-speed memory usage for Mobile Platforms will overtake the PC memory industry by the year 2015. Designing the various bus interfaces in the mobile platform from both a layout and timing perspective requires an understanding of a number of high-speed signal integrity and EMI/EMC issues. The purpose of this course is to discuss high-speed design and EMI/EMC concepts as it applies to mobile platforms. In particular, the concepts learned will be applied to high-speed interfaces such as:

- Mobile DRAM (LPDDRx) Interface
- Mobile PCI Express (M-PCIe) Interface
- Universal Flash Storage (UFS) Interface

This course will instruct you in the disciplines to "do it right the first time." The course will also cover EMI/EMC issues and solutions to build a compliant mobile product that meets timing constraints, minimum cost, and accomplishes "just in time."

You Will Learn:

- Design transmission lines
- Overcome the negative effects of capacitance of the interfacing ICs on the bus
- Minimize crosstalk between/among the high-speed signals
- Bypassing (innerplane and discrete capacitors) and power delivery (the proper energy to the IC pin at the required time)
- Overcome the negative effects of vias: throughhole, blind and buried
- Modify PCB to I/O connector mating to minimize impedance mismatch reflections
- Use digital simulation to achieve signal integrity

Course Length: 3 Days

Who Should Attend the Course?

Digital logic engineers. System Architects, EMC specialists, Technicians, PCB layout professionals, IC designers, Application Engineers, Anyone who works with high-speed digital logic

Course Outline:

Day 1

Fundamentals
Frequency, Time and Distance
Lumped Versus Distributed Systems
Four Kinds of Reactance
Ordinary and Mutual Capacitance & Inductance
EM Fields
Geometry, C, L, & Z_o, interrelationships
C & L Resonance

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High-Speed Properties of Logic Gates/Measurement Techniques
Quiescent vs. Active Dissipation
Driving Capacitive Loads
Input Power and External Power
Intersymbol Interference (ISI), eye diagrams and jitter
Shoot Through Current (SSO) and how to minimize it
Ground Bounce, Lead Inductance, Simultaneous Switching Noise (SSN)
Electronic Packages: QFPs, PGAs, SOIC, PLCC, BGA, COB, TAB, FC, CSP and their relationship to SI
Lead Capacitance and Thermal Considerations
Viewing a Serial Data Transmission System, the eye pattern closure ISI, Skin effect and tan loss.
PLL and DLLs
Observing Crosstalk

Transmission Lines
The quality factor, Q, and why lumped circuits can ring and cause EMI.
Infinite Uniform Transmission Line
Effects of Source and Load Impedance
Determining Line Impedance & Propagation Delay using TDR and VNA
Skin/proximity effect & Dielectric Loss
The Capacitive Load - Z_o and propagation delay
Matching Z_0 with trace alterations (neckdowns) – minimizing the C load
90^0, 45^0 bends – are they concerns?
Even/odd, differential/common modes are their effects on LVDS.

Terminations/Vias
End/Source/Middle Terminators
AC Biasing for End Terminators, where should it be used and how to choose the capacitor
Hairball networks, bifurcated lines and capactive stubs
Terminating differentials – Eliminating common mode and minimizing power
What causes differentials unbalance?
Mechanical Properties of Vias
Capacitance & Inductance of Vias
Return Current and Its Relation to Vias
Through Hole, Blind, Buried, Micro Vias
Intelligent Vias and autorouters
Via discontinuity and via resonance concerns

Ground Planes and Layer Stacking
High-Speed Current Follows the Path of Least Inductance
Crosstalk in Solid and Slotted Ground Planes
Inductive/capacitive ratios for micro strips, striplines, and asymmetric, dual, and edge LVDS
Guard Traces – Do they stop crosstalk, can they resonate?
Near-End and Far-End Crosstalk
Separating analog from ECL/PECL and TTL/CMOS the concept of moats/floats/drawbridge
Split planes - CMOS/TTL, PECL and analog using the same bias voltages
How to Stack Printed Circuit Board Layers (e.g. 4, 6, and 10 layer) for Z_o and crosstalk control, Cu fills on signal layers, minimizing warpage
Interplane Capacitance – How thin? What material? Stackup placement
SIR vs. frequency, software for performing crosstalk and ground bounce tests

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Day 2

Power Systems

Providing a stable Voltage Reference – Cu planes
Distributing Uniform Voltage – Sense lines, bulk C and interplane C
Choosing a Bypass Capacitor – Electrolytic/tantalum and ceramic
Power plane resonance – serial and parallel, how to minimize both
Designing a .1 ohm bypass system up to F_{knee}
Designing for constant ESR
IC die capacitance, discrete C in the IC package
Why the 0201 – Both for better bypassing and EMI control
Minimizing L-Capacitor layouts for SOICs, PLCCs, and various configurations of BGAs

Connectors & Cables
Mutual and Series Inductance – How Connectors Create Crosstalk
and EMI
Using Connectors on a Multidrop Bus (Z mismatch reflection) and how to match Z_c to Z_o
Measuring Coupling in a Connector
Continuity of Gnd Underneath a Connector
Special Connectors for High-Speed requirements – Crosstalk and matching Z_o
Differential Signaling Through a Connector

Buses
Multidrop systems: Drivers
How they function, Clock rates, typical failures
ISI – Minimize the effect with Equalization and Preemphasis
LVDS: types, unbalance, noise, layout & making them function
Methods to speed up busses – Distributive driving and load capacitance matching

Clock Distribution
Timing Margin and Clock Skew
Using Low-Impedance Drivers and Clock Distribution Lines
Source Termination of Multiple Clock Lines
Controlling Crosstalk on Clock Lines
Delay Adjustments – Serpentine traces/DACs and varisters for dynamic delay
Differential Distribution
Controlling Clock Signal Duty Cycle using the integrator
Source synchronous clocking, DDR & RDRAM

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High-Speed Buses and Interfaces

Low Power Dual Data Rate DRAM 3 (LPDDR3)

- DDR Nomenclature – IC level and PCB level
- Column Address (CAS)
- Row Address (RAS)
- Latency and Internal Timing
- DIMM Fly-By Topology
- On-Die Termination (ODT)
- DQ and DQS Timing Requirements
- RDIMM – Advantages for High-Speed R_s & R_t Temperature Compensation Techniques
- Providing On Controller (OCT) R_s & R_t Termination for Transmission Line Matching
- Clock Structure
- CMD and Address Structure
- Address, DM, and CMD Daisy Chain Routing
- Matching Transmission Lines

Differences between UDIMM, RDIMM, and SDRAM will be specified along with design changes between LPDDR2/LPDDR3. A detailed set of layout guides for PCB Designer Engineers for both UDIMMs, and RDIMMs will be provided along with command and address guides for SDRAMs.

Mobile PCI Express (M-PCIe)

- M-PCIe employs a MIPI M-PHY and hence electrical characteristics of M-PCIe will be discussed in this light
- Differential bus will be explained – clock rates, data rates, PLLs, encoding schemes and data transmission overhead
- Differential pair layout guides for microstrip, edge couple and broadside coupled stripline configurations providing the proper trace width, conductor spacing and power/ground layer spacing for ideal high-speed data transfer capability
- Designing the interface for M-PCIe Buses
- Finally the instructor will offer thoughts on the PCIe 4.0 spec (8 GHz clock and 16 GHz data rate) and whether it is possible to design at this frequency.

Universal Flash Storage (UFS)

- UFS employs a MIPI M-PHY and hence electrical characteristics of UFS will be discussed in this light
- PWM & High-Speed Burst Modes
- Mandatory & Optional Data Rates
- Power Supply Requirements
- Differential Signaling for Driver/Receiver
- Clock Parameters
- Charge Pump Capacitors

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Day 3

EMI Concerns of Mobile Platforms

EMI, Source, path and receptor. Why all three must be present to have an EMI problem.
EMI regulations – standards for USA, Europe (EU), and Asia. The course text provides a detailed description of all the test requirements, equipment to conduct the tests and the governing bodies/committees that mandate the tests are provided.
Threats – RFI, ESD, Power Disturbances, Internal
EMI Issues – Frequency, Amplitude, Time, Impedance Dimensions
Conducting an EMI Test – Pre compliance, Compliance Testing, and Post-Audit Testing. What is uncertainty and how does it affect the test plan?
How the Tests Are Conducted—For all the following tests, the hardware instrumentation, the layout, the pass/fail criteria, and tips/techniques to pass the test will be covered. Also, the test site will be defined, i.e. OATS, screen room, anechoic chamber and TEM cell. The step-by-step sequence of how each test is conducted will be detailed.

- Radiated Emissions
- RF Immunity
- ESD

Interference Coupling Mechanism - What is the near/far field, coupling modes, resonance and why are parts placement, proper terminations and grounding so important.
RFI, EMI regarding PCBs, computers, analog designs, and systems
Grounding designs/Filtering – Single ground, modified and multipoint grounding, which one should be used for your design.
CM Radiation – Why is common mode (CM) the major problem versus differential mode (DM)?
Antenna Loops – Why are antenna loops the major cause of radiated emission failures for PCBs?
Basics of PCB Radiation – Why do both lumped and distributive (transmission lines [T.L.]) circuits radiate? Why does a high Q circuit radiate? How do you terminate a T.L. to minimize radiation? What about the capacitive load and why does it cause radiation?
PCB Suppression Techniques – Terminations, filters, and devices – how are they used to suppress radiation?
Design for Immunity – Watchdog timers, offensive/defensive programming, checksum, Hamming, and other techniques. How intelligent software helps pass immunity testing.
Switching Mode Power Supplies (SMPS) – SMPS Chopping Frequency.

- Why is it the major cause of conducted emissions?
- Filters – Schematic configurations of harmonic filters.
- What happens when transients/ESD hits the SMPS mains?
- What are the immunity concerns?
- What are screens and snubbers, and how is a transformer wound?

Picket fences, the 20H rule and Cu fills – What can they do to suppress emissions?
Ideal stackups to be EMC.
Spread Spectrum Clocking – Why does it suppress radiated emissions? Under what conditions can it be used? Is there a better method?
Bypass and Radiation on PCBs – Why use the 0201, Ycap and four terminal cap? Types of innerplane capacitance and does innerplane capacitance help with emissions?
Interference Coupling Modes – Why does ground bounce cause differential and common mode noise and how does that cause emissions?
Near/Far Field - What determines the breakpoint between them and what happens to the characteristic impedance at the breakpoint?
Differential/common coupling modes and resonance – What are the quarter length resonant mode differences when the load impedance is very high versus very low?
Analog circuitry – Transients, filtering, grounding and noise isolation. Opto couplers versus spin resistors; which is better?

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Cables/Connectors Interfaces, Filtering and Shielding

Capacitive and Magnetic Shielding – What is the difference and how should the shield be tied to ground for either case?
Slots – Why do they radiate and is the radiation through them predictable?
Shield Grounding – How should shields be tied to ground to minimize circulation current?
Cable Radiation – Radiation through the shield and at the connector bulkhead connection.
Shielding Types – When do we use Cu and Al versus mu metal, steel, or permalloy?
Transfer Impedance – What is it? Why is it detrimental to shielding, and how is it minimized?
Shielding Connection – Leakage – How to design a non-emission connector to a bulkhead.
Loss of Ground Plane in Cables – Why does it cause crosstalk, radiation, reflections and propagation delay?
Cables Configuration – What shielding/grounding techniques should be used to minimize crosstalk and radiation?
Antenna Loops with Cable Connections – Why do shielding pigtails cause emission non-compliance?
High-Speed Connectors – How are they configured to minimize skin effect, dielectric loss, crosstalk, and radiation?
Filtering – Types of filters, their attenuation capability and how should they be mounted?
Shielding vs Filtering – Cost tradeoffs versus attenuation capability –When should either or be used?
Using Ferrites – Amperes Rule - Why do they work so well for both DM and CM?
Radiation Through Shields – Current density versus skin depth, incident versus reflected fields

Recommended Prerequisites:

Basic knowledge of ICs, high-speed designs and PCB layouts. No advanced math is required though attendees will find it helpful to bring a scientific calculator to the course.

Course materials:

1) Course presentation PDF
2) Optional on request, Textbook: "*High-Speed Digital Design: A Handbook of Black Magic*" by Howard Johnson, Ph.D. and Martin Graham, Ph. D.
3) Optional on request, Textbook: "*EMC for Product Designers*" by Tim Williams