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MIPI I3C Architecture

Training

Let MindShare Bring "MIPI I3C Architecture" to Life for You

MIPI I3C (Improved Inter Integrated Circuit) is a two-wire, medium speed, multi-drop control bus originally intended to connect sensors in mobile devices to a processor. The full I3C communications protocol is defined in the *MIPI I3C Specification* which requires MIPI Alliance membership for access. Another version of the specification, referred to as *MIPI I3C Basic*, is publicly available. Disclosed features of I3C not covered in MIPI I3C Basic Specification are briefly described in the course but the reader is directed to the MIPI Alliance (and the full version of the specification) for complete details. Fortunately, as the two specifications have evolved, MIPI has migrated many of the advanced features into the I3C Basic Specification---attracting more developers and expanding the reach of MIPI I3C into a wider range of embedded and mainstream computer applications.

Many current platforms rely on I2C (Inter Integrated Circuit) and SPI (Serial Peripheral Interconnect) for connecting sensors and other low-medium speed devices to a processor. MIPI I3C addresses long-standing limitations of both of these protocols and provides a path towards consolidating legacy interfaces into a single connection type that leverages positive features of I2C/SPI while adding new capabilities that are important as more diverse device types are supported. At the same time, MIPI I3C SDR is an enhanced version of I2C and backward compatibility is a requirement.

Another feature that should promote I3C acceptance is the *MIPI I3C Host Controller Interface (HCI) Specification*. This specification standardizes host interactions with I3C devices using two operational modes: DMA and PIO. HCI DMA mode is important in larger systems that have the memory resources to support host controller models similar to those used by USB xHCI and NVMe to off-load the CPU from much of the burden of managing device transactions. On the other hand, an I3C host controller operating in PIO mode may be better suited to an embedded system where logic, memory, and power resources are more scarce and a microcontroller may be responsible for managing the I3C controller and all of its attached devices.

You Will Learn

- Major features defined in the MIPI I3C Basic Specification
- How MIPI I3C addresses some of the long-standing speed, power, and pin count limitations of alternative IC communication protocols, including I2C and SPI
- Why I3C devices dynamically switch data drivers between push-pull and open drain signaling
- The motivations for MIPI I3C Hot-Join in power sensitive applications
- How I3C compliant devices report bus and internal characteristics to software
- How an enhanced set of direct and broadcast Common Command Code (CCC) transactions help simplify initialization, changing bus modes, and with device control and status operations
- The use of I3C in-band interrupts (IBI) to reduce pin count and enable devices to send critical status information as part of the IBI payload.
- Key features of the MIPI I3C Host Controller Interface (HCI) Specification

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Who Should Attend?
This MindShare course is designed for hardware/software engineers and others needing detailed coverage of MIPI I3C protocol.

Course Length: 3 Days

Course Outline:

- Key Specifications
  - MIPI I3C Specification and the MIPI I3C Basic Specification
  - MIPI I3C Host Controller Interface (HCI) Specification
- I3C Background & Overview of Key Features
  - Limitations of I2C/SPI protocols and I2C features carried forward into I3C
  - I3C bus topology: controllers, targets, routers, bridges
  - Default two-wire half-duplex signal interface and the multi-lane data option
  - Dynamic switching between open-drain and push-pull data signaling
  - Interleaved protocols: I3C Single Data Rate (SDR), High Data Rates (HDR), legacy I2C
  - Standardized configuration model
  - Static, dynamic, and group addresses
  - Private read/write and Common Command Code (CCC) transactions
  - Improved bus error detection, reporting, and recovery
  - In-band Interrupts (IBIs) replace external interrupts
  - Hot-join capability enables devices to be added after bus configuration
- Device Capability Discovery
  - Required and optional feature support
  - I3C characteristics registers and I2C Legacy Virtual Register (LVR)
  - Accessing device capabilities and advanced capabilities
- Bus Communications Basics
  - Private read/writes and Common Command Code (CCC) messages
  - Introduction to default SDR protocol: controller and target roles
  - Inactive bus conditions: idle, available, free
  - Motivations for dynamic switching between open drain and push-pull signaling
  - I3C broadcast address and arbitration events
  - Bus Activity states for power conservation
- I3C Single Data Rate (SDR) Message Details
  - Private read/write transfer examples
  - Direct and broadcast CCC message examples
  - Managing maximum read length (MRL) and maximum write length (MWL)
  - Programming and using group addresses
- Bus Initialization and Dynamic Address Assignment (DAA)
  - Motivations for DAA; reducing conflicts, IBI priority, hot-join support
  - After reset/power-up: static addresses and PIDs
  - Key CCC messages used for DAA
  - Hot-join and DAA
- Hot-Join Mechanism
  - Motivations
  - In-band reset vs. sideband wake events
  - Hot-join arbitration and request sequence
  - Dynamic address assignment for newly discovered devices

- In-band interrupts (IBI)
  - Reporting IBI capabilities
  - Dynamic address and IBI priority
  - IBI arbitration sequence & controller acceptance/deferral
  - Mandatory data byte (MDB) and payload options
  - Enabling and disabling target interrupts
- Secondary Controllers
  - Primary and secondary controller roles
  - Checking for secondary controller capabilities
  - Secondary controller request
  - Primary to secondary controller handoff sequence
  - Controllers passing target address and capability information using CCCs
- HDR-DDR Protocol
  - Target reporting of HDR-DDR support
  - HDR vs. SDR clocking
  - Transition from SDR mode into HDR-DDR mode
  - Word-based HDR-DDR commands, data, CRC
  - Preamble and parity bits
  - HDR Restart and Exit patterns
- HDR-BT Protocol
  - Motivations and advantages of I3C HDR-BT protocol
  - HDR-BT mode entry and exit
  - Block-based messages
  - CRC-16 vs. CRC-32
  - Transaction examples
  - Managing payload size (maximum read/write length)
- Multi-Lane Data Transfers
  - Discovering capabilities and configuring dual-lane, quad-lane transfers
  - Maintaining interoperability with single-lane devices
  - Multi-lane SDA striping and DDR clocking
  - Frame coding
- MIPI I3C Host Controller Overview
  - Motivations and goals for MIPI I3C HCI (Host Controller Interface)
  - Host connection: PCIe bus vs. others
  - PCI Registers and MMIO Capability, DAT/DCT register sets
- HCI PIO Mode Operations
  - PIO mode registers and internal queues/ports
  - Command types and descriptor formats
  - Managing queue thresholds
  - PIO mode masking of interrupt status and interrupt delivery
- HCI DMA Mode Operations
  - Memory ring bundles
  - MMIO ring headers
  - Command ring transfer descriptors and response ring descriptors
  - Ring enqueue and dequeue pointers
  - Data buffers: standard and scatter-gather pointers
  - DMA mode I3C bus transfer example

Recommended Prerequisites

Some background in serial bus protocols such as I2C and SPI is helpful.

Course Material:

Downloadable PDF version of the presentation slides