Comprehensive Intel Core 2 (Penryn) Processor and Chipset Combo Course

Training

Let MindShare Bring “Intel Processors and Chipsets” to Life for You
The Core 2 Penryn processor is the latest released member of Intel’s IA32 family. As with its predecessors, it is backward compatible with the first 32-bit CPU, the 80386. Each IA32 processor brought new hardware and software features, and Penryn continues the focus of the current generation core architecture processors on providing high performance at the lowest possible power. Penryn’s new 45nm microarchitecture enables greater hardware integration, including a 50% increase in the Level 2 cache size over earlier 65nm Core 2 processors. Penryn includes CPU models targeting laptop, desktop, and workstation/server platforms; new hardware and aggressive power management capabilities allow better tuning of power consumption/performance to suit the application.
Penryn processors support the standard x86 operating modes, registers and instruction set, interrupts, and CPU virtualization. In addition, the processor package includes an interface to Intel’s parallel Front Side Bus (FSB). This bus features quad-pumped data rates and is the same FSB as is used by several of Penryn’s immediate predecessors; for this reason, Penryn is compatible with many of the same platform chipset components.

The Chipset is at the heart of a PC motherboard. It is a computer chip or set of chips which interconnects the processor to various subsystems of a PC which includes system DRAM memory, graphics and peripheral devices on such interconnects as USB, SATA, IDE, Ethernet, PCI/PCI Express, LPC, SMBus etc links. This course dissects the Chipset into its subunits and explains each subunit. In doing so, you will understand modern PC architecture.

You Will Learn:
- How a PC works
- Penryn’s place in the IA32 CPU family
- Penryn platform variations
- CPU Operational Modes
- Penryn internal Hardware and Software Architecture
- Processor Initialization and Start-Up
- Front Side Bus features
- Power and Thermal Management
- X86 Interrupts
- The role of a processor, system memory and peripherals
- How a variety of interconnect buses such as PCI Express, USB, SATA work
- Communication process between processor, peripheral devices and memory via the chipset
- Improve your PC board debug skills
- The basics required to understand detailed architecture of processor and a variety of IO buses
- What’s next: a preview of upcoming Nehalem CPU features

Course Length: 5 Days

Who Should Attend?
This course is hardware-oriented. It is however suitable for both hardware and software engineers. The course is ideal for system board-level design engineers who need a broad understanding of the Processor, PC and chipset architecture. It is suitable for chipset design engineers and processor validation engineers. Software engineers will understand how to access configuration space.
Course Outline:

Intel Core 2 (Penryn) Processor Topics

- IA32 CPU and Platform Background
  - IA32 Family and Penryn CPU
  - Intel Platform Basics
  - Penryn CPU Internal Architecture Introduction
- Processor Internal Architecture Details
  - Baseline Registers and Instruction Set
  - Real Mode Segmentation
  - Protected Mode Segmentation
  - Demand Mode Paging
  - The Flat Segmentation and Paging Model
  - IA32e 64 bit Extensions
  - Penryn Caching Topics
  - Penryn Microarchitecture
- Processor Initialization
- CPU Management Topics
  - Power Management
  - CPU Thermal Management
  - Machine Check Architecture (MCA)
  - System Management Mode (SMM)

Intel Chipset Topics

- Role of the chipset in the system
- Current chipset architecture overview
- Memory and IO mapping and chipset address decoding
- Configuration address space and transaction generation
- MESI cache coherency and snooping protocol
- Communication model between various devices through the chipset including multi-processor communication via the Front-Side-Bus (FSB)
- Interfaces related to Memory Controller Hub (MCH) including FSB, DRAM bus, PCI Express, DMI and clock interfaces
- Interfaces related to IO Controller Hub (ICH) including USB, SATA, IDE, LPC, SMBus etc.
- Interrupt Handling in Chipset and Processor
- Overview of MCH and ICH configuration register map
- Review of a variety of server, workstation, desktop and notebook chipsets
- Nehalem CPU and Platform Preview (based on preliminary information)

Recommended Prerequisites: Basic understanding of Computer Architecture

Course Material:

MindShare Presentation: **Hardcopy and Softcopy of Comprehensive Intel Core 2 (Penryn) Processor and Chipset Combo Course materials**

Author: Tom Shanley
Publisher: Addison Wesley
Available through the MindShare Store and major bookstore outlets.
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