

## Comprehensive Intel® QuickPath Interconnect Architecture

### Training

#### Let MindShare Bring “Intel® QuickPath Interconnect (Intel® QPI)” to Life for You

The modern PC architecture will be revolutionized with the advent of Intel's latest generation of Nehalem and Tukwila processors. Communication bottlenecks between processors as well as between the processor and chipset will be eliminated with the replacement of the former processor bus (commonly referred to as the Front-Side Bus or FSB) with the latest generation high-speed, low-latency point-to-point Intel QuickPath Interconnect. This new inter-processor and processor-chipset interconnect will allow for seamless integration and connection of one or more processors (such as in server platforms) with the chipset.

#### You Will Learn:

- Benefits of Intel QPI over previous generation processor buses
- Fundamentals of the Intel QuickPath Interconnect protocol
- Coherent and non-coherent communication model
- Link Initialization
- System Initialization
- Interrupt support, error handling, power management
- Electrical signaling

**Course Length:** 3 days

#### Who Should Attend?

This course is hardware-oriented. It is however suitable for both hardware and software engineers. The course is ideal for engineers who need a broad understanding of the processor-to-processor and processor-to-chipset interconnect on Intel Nehalem and Tukwila processors. The course is suitable for chipset design engineers and processor validation engineers. Software/firmware engineers will come away with a good understanding of some of the main responsibilities of BIOS in a QPI-based system.

#### Course Outline:

- Intel QPI Overview
  - Historical Perspective: Intel Front-Side-Bus (FSB) and platform architecture
  - Intel QPI features
    - Performance
    - Packets, Flits, Phits
  - Platform architecture based on processors with Intel QPI
    - Single-, Dual-, Quad- and Larger- processor systems
  - Overview of layered architecture in QPI interface design
    - Agents, Nodes, Addressing, Routing
    - Channels / Virtual Networks / Virtual Channels
    - Cache coherency examples with Intel QPI
- Interconnect Layer Details
  - Protocol Layer and Address Decode
    - Source and Target Address Decoding
    - Transaction IDs

- Protocol Channels
- Routing Layer
  - NodeID / QPI Link / Virtual Network mapping
- Link Layer
  - Header packets / Data packets
  - Header contents
  - Flow Control
  - Ack / Retry processes
- Physical Layer
  - Link Initialization
  - Reset
  - Link Self-healing
  - Link Retraining
- Protocol Details
  - Coherent Protocol Details
    - MESIF cache coherency protocol
    - QPI Request / Writeback / Snoop / Snoop Response / Data Response messages
    - Source Snooping behavior
    - Home Snooping behavior
    - Mixed (Home and Source) Snooping behavior
  - Non-Coherent Protocol Details
    - MMIO traffic
    - IO traffic
    - Configuration traffic
    - Peer-to-Peer traffic
    - Non-Coherent Message transactions
    - “Bus” Locking
- Additional Topics
  - Interrupt Delivery
    - Background
      - Advanced Programmable Interrupt Controllers (APICs) & APIC IDs
      - Physical, Flat, Cluster destination modes
      - Redirection (Lowest-Priority Mode)
    - QPI Interrupt messages and interrupt mapping
  - Power Management
    - Link Power Management (L0s, L1)
    - Platform Power Management
  - Fault Handling
  - Design For Test (DFT) and debug
  - Electrical Specifications

### **Recommended Prerequisites:**

A basic understanding of computer architecture.

### **Training Materials:**

Students will be provided with a softcopy of presentation material used in class. (Hardcopy can be provided upon request.)