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Comprehensive MIPI M-PHY Architecture

Training

Let MindShare bring "MIPI M-PHY Architecture" to life for you

The MIPI M-PHY standard is utilized in the following bus architectures: UFS (Universal Flash Storage), M-PCIe, SSIC (SuperSpeed Inter-Chip), CSI-3 (Camera Serial Interface) and DigRF v4 (Digital RF standard for LTE/WiMax interface). Knowledge gained in this short course can be utilized towards understanding the physical layer design associated with UFS, M-PCIe, SSIC, CSI-3 and DigRF.

You Will Learn:

- How to design a MIPI M-PHY
- Basics if 8b/10b protocol
- Test Modes to design-in that allow for testability
- Transmitter and Receiver electrical characteristics.

Who Should Attend?

This course emphasizes the hardware architecture. The course is ideal for RTL-, chip-, system- or system board-level design engineers who need a broad understanding of MIPI M-PHY design.

Course Length: 2 Days

Course Outline:

M-PHY Logical

- Definitions
- Signalling
- 8b/10b, Framing and Scrambling
- Module State Machines
- Configuration
- Test Modes

M-PHY Electrical

- M-TX Characteristics
- M-RX Characteristics
- Electrical Interconnect
- Interface

Optical Media Converter

- Architecture
- Electrical
- Configuration
- Test

Protocol Interface

- TX and RX DATA SAP
- TX and RX CTRL SAP
- Attributes

Recommended Prerequisites:

A basic understanding of digital bus architectures is highly recommended.

Course Material:

Downloadable PDF of the presentation slides.