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Hands-On Mobile PCI Express (M-PCIe) Architecture

Training

Let MindShare Bring "Hands-On Mobile PCI Express (M-PCIe) Architecture" to Life for You

M-PCIe is a high-performance I/O bus used to interconnect peripheral devices in mobile platforms. It's predecessor, PCIe, has been designed into many types of platforms, and has established itself as the bus of choice for on-board I/O connections. The mobile version largely replaces the PCIe Physical Layer with the MIPI M-PHY to achieve better power conservation. This architecture is governed and defined by the PCISIG (Peripheral Component Interconnect Special Interest Group), but uses the M-PHY spec published by the MIPI Alliance.

MindShare's M-PCIe Architecture course starts with a high-level view of the design that gives the big-picture context and then drills down into the details for each part of the design, providing a thorough understanding of the hardware and software protocols.

M-PCIe changes the physical layer to support the M-PHY model, adding some new steps to the link training process and defining a new initialization protocol. The good news is that the upper layers are left unchanged.

You Will Learn:

- PCI Express features and capabilities
- The definition and responsibilities of each of the layers in the interface
- How Link-level automatic error detection and correction works
- The levels of error detection and reporting
- Details of the packet-based protocol used by PCIe
- Address space and packet-routing methods
- How the various power management techniques work
- Details of the configuration registers that give software visibility and control including new M-PCIe registers
- Changes to the Link Training & Initialization model to support the M-PHY
- How the M-PHY MODULE state machines work
- The RRAP model of device discovery
- How M-PCIe achieves much lower power consumption compared to PCIe

Who Should Attend?

This course is hardware-oriented, but is suitable for both hardware and software engineers because the configuration registers used to control the hardware are covered in detail. The course is ideal for RTL-, chip-, system- or system board-level design engineers who need a broad understanding of M-PCIe. Because the course contains practical examples of transactions on the various bus interfaces, the course is also suitable for chip-level and board-level validation engineers.

Course Length: 4 Days (but customizable to shorter duration)

Course Outline:

- PCI Express Features and Architecture Overview
  - Layered Architecture
  - TLP, DLLP and Ordered Set Packet Format Overview
  - Protocol Overview
- Configuration Overview
  - Legacy and Enhanced Configuration Transaction Generation

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  - Header 0/1, Capability and Extended Capability Register Overview
  - Bus Enumeration
  - **Arbor Lab**: Scan your system and determine topology
- Address Space and Transaction Routing
- TLP Format Details
- Quality of Service (QoS) Overview
- Flow Control
  - Initialization
  - Runtime Update Mechanism
- Transaction Ordering
  - Simplified ordering table (2.1)
  - ID-Based ordering (2.1)
- DLLP Format Details
- ACK/NAK Protocol
  - Error Recovery Mechanism
  - Examples of Variety of Error Scenarios
  - Nullified Packets – Store-and Forward vs. Cut-Through Mode
- Physical Layer Logic Overview (Gen1/Gen2/Gen3)
  - Clock Recovery
  - Byte Striping
  - Scrambling
  - 8b/10b Encoding
  - 128b/130b Encoding
- M-PHY Details
  - Electrical
  - De-emphasis
  - Module State Machines
  - M-TX and M-RX characteristics
  - Reference M-PHY Interface (RMMI)
  - M-PCIe related new configuration registers
- M-PCIe Link Initialization & Training
  - Detect, Polling, Configuration, L0, Recovery (Re-training) States
  - Link Power Management States
  - Modifications for M-PCIe
    - New LTSSM and Training changes
    - Initialization and discovery
    - Remote Register Access Protocol (RRAP) and Remote Register Configuration (RRC)
    - Link Width and Speed Changes
- Error Detection and Handling
  - Correctable, Non-Fatal and Fatal Errors
  - **Arbor Lab**: Determine source and error reporting mechanism
- Power Management
  - Software initiated Power Management
  - Hardware initiated Power Management
  - M-PCIe power-conserving concepts
- Interrupt Support
  - Legacy Interrupt Handling
  - MSI and MSI-X
  - **Arbor Lab**: Investigate source of MSI interrupt and delivery
- System Resets
  - Fundamental Reset (Cold and Warm Reset)
  - In-band Reset (Hot Reset)
  - Function Level Reset (FLR)

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Recommended Prerequisites:

A basic understanding of digital bus architectures such as PCI is highly recommended.

Course Material:

1) PCI Express Technology eBook (or hardcopy on request) by Mike Jackson and Ravi Budruk.
2) Downloadable PDF version of the presentation slides.
3) MindShare Arbor software tool, used for student labs in the class.
4) Optional: Comprehensive PCI Express 2.0 eLearning course (discounted pricing applies)
5) Optional: PCI Express 2.1 and 3.0 Update eLearning course (discounted pricing applies)
6) Optional: Intro to PCI Express IO Virtualization eLearning course (discounted pricing applies)