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Mobile DRAM (LPDDRx) Architecture Course Info

Let MindShare Bring "Mobile DRAM (LPDDRx) Architecture" to Life for You

Ever since Intel introduced DRAM memory, it has evolved in size, density, speed and architecture. It has also evolved in power consumption, most notably with the Low-Power DDRs. MindShare's Mobile DRAM (LPDDRx) Architecture course describes the development of mobile memory systems and covers in-depth today's most advanced DRAM technology. The course ultimately focuses on ultra-dense, high-speed LPDDR3/LPDDR4 technology. Memory cell theory, operation, and key chip architecture differences from LPDDR1 through LPDDR4 are covered. Initialization of a memory channel is described. System design challenges, ranging from signal routing to error handling, are covered. Using waveform examples, state diagrams and truth tables, the commands and correct sequencing of operations are taught. DRAM controller design principles are also discussed.

You Will Learn:

- How a DRAM array is organized
- How to understand DRAM transaction waveforms so that you can debug a memory channel
- How to refresh a DRAM
- How to initialize and train a DRAM channel
- Electrical characteristics of LPDDRx signals
- Elements of DRAM controller design
- Differences between LPDDR1 through LPDDR4
- DRAM power management

Course Length: 2 Days

Who Should Attend?

This course is hardware centric but does describe DRAM memory and DRAM controller initialization. It is suitable for hardware engineers, but software/firmware engineers will benefit. The course is ideal for DRAM controller designers, chipset designers, system board-level design and validation engineers.

Course Contents:

- System Architecture
  - PC Platform Architecture
  - NUMA Architecture
  - Mobile SoC Architecture
- Back to the Future DRAM Intro
  - It's more similar than it is different
- DRAM Cell Architecture
- DRAM Device Architecture
  - LPDDR2, LPDDR3, LPDDR4, and WideIO
- PC DDRx/LPDDRx Feature Summary, Comparison, and Roadmap
  - LPDDR4 New Features and Comparison to LPDDR3
- DRAM Controller Basics
  - Block Diagram
  - What is the address?
- Packaging LPDDR3, LPDDR4, WideIO
  - Monolithic
  - Stacked Die
  - Package-on-Package
  - Dual LPDDR4 Channels
  - WideIO Stack
- Device Pin Descriptions

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    - LPDDR3
    - Radical LPDDR4 Changes Due to Channels and LVSTL
- Commands and Waveforms
    - LPDDR3
    - Radical LPDDR4 Changes Due to Channels and LVSTL
- Refresh
    - Auto Refresh
    - Self Refresh
    - Auto Self Refresh
    - Per-Bank Refresh
    - Row Hammer and LPDDR4 Target Row Refresh
- Electrical Specifications
    - LPDDR3 HSUL
    - LPDDR4 LVSTL
    - Comparison to DDR3 SSTL and DDR4 POD
    - IDD
- Power Management
    - Active and Precharge Power Down
    - LPDDR3 Deep Power Down
    - Self Refresh, Temperature Compensated
    - Clock Throttling
- Introduction to Signal Integrity Issues
- Signal Routing
- On-Die Termination
    - LPDDR3 Data Group ODT
    - LPDDR4 Command Bus ODT
- Initialization, Calibration, and Training
    - JEDEC Initialization
        - Mode Registers
        - Initialization
    - Calibration and Training
        - ZQ Calibration
        - Data Training / DQ Cal. / Read Cal.
        - Write Leveling
        - CA Training / Command Bus Training
        - LPDDR4 Internal Vref
- Errors and Error Handling
    - Sources of Errors
    - Hard Errors and Soft Errors
    - Internal Errors and External Errors
    - LPDDR4 Post Package Repair
    - ECC as Intro to Device Internal ECC
- Introduction to Testing
    - DRAM Functional Tests
    - DRAM Parametric (pin) Tests
    - Controller Functional Tests
    - Controller Parametric Tests

Recommended Prerequisites:

A basic understanding of digital logic.

Course Material:

Students will be provided with soft-copy of presentation material used in class