DRAM (DDRx/LPDDRx) Architecture

Training

Let MindShare Bring “DRAM (DDRx/LPDDRx) Architecture” to Life for You

Ever since Intel introduced DRAM memory, it has evolved in size, density, speed and architecture. DRAMs have evolved to DDR4 and LPDDR3 DRAMs. MindShare’s DRAM Technology Architecture course describes the development of computer memory systems and covers in-depth today’s most advanced DRAM technology. The course ultimately focuses on ultra-dense, high-speed DDR3/DDR4/LPDDR2/LPDDR3 technology. Memory cell theory, operation and key chip architecture differences from SDRAM through DDR4 as well as LPDDR1 through LPDDR3 is covered. The PC DIMM organization is covered, as well as bus implementations. Initialization of a memory module is described. System design challenges, ranging from signal routing to error handling, are covered. Using waveform examples, the commands and basic differences between DDR3 and DDR4 as well as LPDDR2 and LPDDR3 are taught. DRAM controller design principles are also discussed.

You Will Learn:
- How a DRAM cell is organized
- Organization of a variety of memory modules
- How to understand DRAM transaction waveforms so that you can debug a memory channel
- How to refresh a DRAM
- Electrical characteristics of DDRx and LPDDRx signals
- Elements of DRAM controller design
- Differences between DDR1 through DDR4 as well as LPDDR1 through LPDDR3
- DRAM power management issues
- Error handling

Course Length: 3 Days

Who Should Attend?
This course is hardware centric but does describe DRAM memory and DRAM controller initialization. It is suitable for hardware engineers, but software/firmware engineers will benefit. The course is ideal for DRAM controller designers, chipset designers, system board-level design and validation engineers.

Course Contents:
- System Architecture
  - PC Platform Architecture
  - NUMA Architecture
  - SoC Architecture
- Back to the Future DRAM Intro
  - It's more similar than it is different
- DRAM Cell Architecture
- DRAM Device Architecture
  - SDRAM thru DDR4
  - DDR4 Bank Groups
  - LPDDR2, LPDDR3, and WideIO
- DDRx/LPDDRx Feature Summary, Comparison, and Roadmap
  - LPDDR3 New Features
  - DDR4 New Features
  - GDDR5 Overview
• DRAM Controller Basics
  - Block Diagram
  - What is the address?
• Packaging DDR3, DDR4, LPDDR3, WideIO
  - Monolithic
  - Stacked Die
  - WideIO Stack
  - 3DS Hypercube
  - Package-on-Package
  - Stacked Package
• DDR3 and DDR4 Module Architecture
  - UDIMM
  - RDIMM
  - LRDIMM
• Device and Module Pin Descriptions
  - DDR3, DDR4
  - DIMM
  - LPDDR2, LPDDR3
• Commands and Waveforms
  - DDR3, DDR4
  - LPDDR2, LPDDR3
• Timing Issues
  - DDR3 and DDR4 DLL for Multi-rank
  - LPDDR2 and LPDDR3 Single and Dual Rank HSUL
  - Derating and Margining
• Refresh
  - Auto Refresh
  - Self Refresh
  - Auto Self Refresh
  - Fine Granularity Refresh
  - Self Refresh Abort
  - Fast Exit Self Refresh
• Electrical Specifications
  - LPDDR2 and LPDDR3 HSUL
  - DDR3 SSTL
  - DDR4 POD
  - IDD
• Power Management
  - Power Down
  - LPDDR Deep Power Down, DDR4 Max Power Saving Mode
  - Self Refresh, Temperature Compensated
• Introduction to Signal Integrity Issues
• Signal Routing
  - Trace-length matching
  - DDR3/DDR4 Fly-by Routing
  - DDR3 On-DIMM Address Mirroring
• On-Die Termination
  - DDR3 and DDR4 Dynamic ODT
  - Sync/Async ODT
  - DDR4 Park Mode
• Initialization, Calibration, and Training
  - JEDEC Initialization
    - DDR3, DDR4, LPDDR3 Mode Registers
- DDR3, DDR4 Initialization
- LPDDR3 Initialization
  - Calibration and Training
    - ZQ Calibration
    - Data Training / DQ Cal. / Read Cal.
    - Write Leveling
    - LPDDR3 CA Training
    - DDR4 Geardown Mode
    - DDR4 Internal Vref for DQ
- Errors and Error Handling
  - Sources of Errors
  - DIMM ECC
  - DIMM Parity
  - DDR4 CA Parity
  - DDR4 Write CRC
  - Multi-Purpose Register
  - MRS Readout
- Testing
  - DRAM Functional Tests
  - DRAM Parametric (pin) Tests
  - Controller Functional Tests
  - Controller Parametric Tests
  - DDR4 Connectivity Test Mode
- Optional Topics
  - SMBus Overview
  - NVM Transaction Overview

**Recommended Prerequisites:**
A basic understanding of digital logic.

**Course Material:**
Students will be provided with soft-copy of presentation material used in class