

NVMe 1.3 Architecture Training

Let MindShare bring “NVMe 1.3 Architecture” to life for you

MindShare's NVMe (Non-Volatile Memory Express) course begins with a review of PCI Express (PCIe) basics as a foundation for the study of NVMe. Next, a high-level view of the architecture provides the big-picture context. Finally, we drill down into some details for each part of the design, providing an introduction to the hardware and software protocols.

You Will Learn:

- An overview of PCIe configuration
- Basics of the NVMe Host Controller Interface model
- The steps for device initialization
- How command queues are set up and managed
- How host software
 - Informs the controller of new commands to execute
 - Learns that commands have been completed
- What commands are defined, and how they work
- Error reporting structures defined
- Power management options

Who Should Attend?

This course is hardware-oriented, but is suitable for both hardware and software engineers because the registers used to control the hardware are described in detail. The course is ideal for RTL-, chip-, system- or system board-level design engineers who need a broad understanding of NVMe.

Course Length: 1 Day

Course Outline:

- Basics
 - PCIe Background
 - Memory addresses and DMA operation
 - IO addresses and Legacy Endpoints
 - Configuration
 - Interrupts
 - Introduction to the Host-Controller Interface model
 - Overview of NVMe operation
 - **Hands-on Arbor lab: discover register addresses**
 - Queue Management
 - Doorbell register operation
 - Tracking completion Phase Tag status
- Commands
 - NVMe Admin Commands
 - NVMe IO Commands
 - Command execution
 - Identify commands
 - Create and delete Queues
 - Priority and Arbitration of commands
 - Use of non-contiguous buffer space
 - Completing commands
 - Informing the Host of completions
 - Asynchronous Event Notification
 - **Hands-on Arbor lab: read commands from a queue**

- NVMe IO Commands
 - Setting up a data buffer
 - Command arbitration
 - Buffer addressing modes (PRPs vs. SGLs)
 - Get Features / Set Features – full coverage of features
- **Hands-on Arbor lab: use of get/set features – discover queue allocation**
- Architecture
 - Error reporting, Error Reporting Structures
 - Firmware updates
 - Controller registers
 - Controller initialization
 - Power Management
 - Reservations
- Appendices
 - Summary of changes for 1.2.1
 - Identify Controller data – new fields
 - Use of NVM Qualified Name (NQN)
 - Keep Alive command added to support NVMe-oF
 - Extensions for HostID, Reservation Report, Get Log Page
 - Summary of changes for 1.3
 - Motivation for changes
 - Boot partitions
 - Thermal management by host
 - Write streams
 - Deallocation
 - Virtualization support
 - Debug support – Telemetry
 - Self-test options
 - Sanitize command
 - Other NVMe commands
 - PCIe Architecture Overview

Course Material:

A downloadable PDF version of the presentation slides
Arbor software

Recommended Prerequisites:

Previous exposure to PCIe is very helpful, as is some general knowledge of PC architectures.