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NVMe 1.4 Architecture Training

Let MindShare bring "NVMe 1.4 Architecture" to life for you

MindShare's NVMe (Non-Volatile Memory Express) course begins with an optional review of PCI Express (PCIe) basics as a foundation for the study of NVMe. Next, a high-level view of the architecture provides the big-picture context of the hardware architecture and software interactions. Finally, we drill down into details for each aspect of the NVMe architecture.

You Will Learn:

- Basics of the NVMe Host Controller Interface model
- The steps for device initialization
- How command queues are set up and managed
- How host software
  - Informs the controller of new commands to execute
  - Learns that commands have been completed
- What commands are defined up to 1.4 spec, and how they work
- Error reporting structures
- Power management options
- Optional PCIe architecture overview on request

Who Should Attend?

This course is hardware-oriented, but is suitable for both hardware and software engineers because the registers used to control the hardware are described in detail. The course is ideal for RTL-, chip-, system- or system board-level design engineers who need a broad understanding of NVMe.

Course Length: 2 Days

Course Outline:

Basic Topics (Covered on Day 1)

- Introduction
  - PCIe Overview
  - NVMe concepts and definitions
  - Comparison with SATA
  - NVMe Host-Controller Interface overview
  - **HANDS-ON ARBOR LAB:** discover register addresses
  - Queue Management
    - Doorbell Head and Tail registers
    - Execution sequence
    - Tracking completion status
- Commands
  - NVMe Admin Commands
    - General Structure of commands
    - Identify command options and results
    - Creation and management of Queues
    - Asynchronous Event Notification
  - **HANDS-ON ARBOR LAB:** View commands in a queue
  - NVMe IO Commands
    - Read and Write command structure
    - Optimizing write commands
    - Avoiding write amplification
    - Buffer addressing modes (PRPs vs. SGLs)
    - Priority and Arbitration of commands

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        - Completing commands
        - Handling Metadata (DIF/DIX)
        - Get Features / Set Features – full coverage of features
    - **HANDS-ON ARBOR LAB:** View get/set features commands, discover queue allocation
- Architecture
    - Error reporting, Error Reporting Structures
        - Asynchronous Events
        - Completion status
        - Log pages
    - Other log pages
    - Firmware updates
    - Controller registers
    - Controller initialization
    - Power Management
    - Reservations

Additional Topics (Requires a 2-day course)

- Summary of changes for 1.3
    - Boot partitions
    - Thermal management by host
    - Write streams
    - Deallocation
    - Virtualization support
    - Debug support – Telemetry, initiated by host or device
    - Self-test options
    - Sanitize command
    - New commands
- Summary of changes for 1.4
    - NVM Sets
    - I/O Determinism
    - Read recovery levels
    - Persistent Memory Region (PMR)
    - Asymmetric Namespace Access (ANA)
    - Namespace write protect
    - Persistent event log
    - Rebuild assist
    - Endurance groups
    - I/O Performance and Endurance Hints
    - Traffic-based Keep Alive
    - Vendor-specific UUIDs
    - Verify - new command
    - Administrative controller
    - SQ Associations
- Other commands
    - Write uncorrectable
    - Write zeroes
    - Compare
    - Dataset management
- PCIe Architecture Overview
    - Introduction
    - Basic operation
    - Transaction types
    - Layers and responsibilities overview
    - Configuration overview

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Course Material:

1) A downloadable PDF version of the presentation slides
2) Optional Add-On: Arbor software
3) Optional Add-On: NVMe eLearning

Recommended Prerequisites:

Previous exposure to PCIe is very helpful, as is general knowledge of PC architectures.