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Hands-On PCI Express 3.1 Architecture

Training

Let MindShare Bring "Hands-On PCI Express 3.1 Architecture" To Life For You

The PCI Express (PCIe) architecture is a third-generation, high-performance I/O bus used to interconnect peripheral devices in computing and communication platforms. PCI Express has been designed into consumer and high-end PCs, embedded computing, and communication markets and has established itself as the bus of choice for on-board I/O connections. This architecture is governed and defined by the PCISIG (Peripheral Component Interconnect Special Interest Group).

MindShare's PCI Express System Architecture course starts with a high-level view of the design to provide the big-picture context and then drills down into the details for each part of the design, providing a thorough understanding of the hardware and software protocols.

The course describes additional features added to the architecture when moving from PCIe specification revision 1.1 to 2.0 to 2.1 to 3.0 . PCIe 3.0 (Gen 3) doubles the bandwidth available in revision 2.0 (Gen 2) by increasing the transfer rate and dropping 8b/10b encoding. But a number of protocol changes were also implemented in the change from revision 2.0 to 2.1, and those are described, too. The Gen 3 changes are physical layer updates to support the higher speed and some new steps that were needed for link training to get that speed working reliably, but the upper layers are left unchanged.

You Will Learn:

- PCI Express features and capabilities
- The definition and responsibilities of each of the layers in the interface
- How the hardware-based automatic error detection and correction mechanism works
- The various additional levels of error detection and reporting
- The details of the packet-based protocol used by PCIe
- The address space and packet-routing methods used
- How the various power management techniques work
- The details of the configuration registers that provide control and status visibility to software
- What are some ECNs related to PCI Express 2.1 and 3.1 specification
- What changes are needed to run the link at 8.0GT/s (rev 3.0 speeds)

Who Should Attend?

This course is hardware-oriented, but is suitable for both hardware and software engineers because the configuration registers used to control the hardware are covered in detail. The course is ideal for RTL-, chip-, system- or system board-level design engineers who need a broad understanding of PCI Express. Because the course contains practical examples of transactions on the various bus interfaces, the course is also suitable for chip-level and board-level validation engineers.

Course Length: 5 Days (but customizable to shorter duration)

Course Outline:

- PCI Architecture Background Foundation
  - PCI Legacy Configuration Transaction Generation
- PCI Express Features and Architecture Overview
  - Layered Architecture
  - TLP, DLLP and Ordered Set Packet Format Overview
  - Protocol Overview
- Configuration Overview
  - Legacy and Enhance Configuration Transaction Generation
  - Header 0/1, Capability and Extended Capability Register Overview

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  - Bus Enumeration
  - **HANDS-ON ARBOR LAB**: Scan your system and determine topology
- Address Space and Transaction Routing
  - Switch Routing Mechanism
  - **HANDS-ON ARBOR LAB**: Debug problem with plug-and-play address mapping
- TLP Format Details
- Quality of Service and Arbitration
  - TC/VC Mapping and VC/Port Arbitration
- Flow Control
  - Flow Control Initialization
  - Runtime Flow Control Update Mechanism
- Transaction Ordering
  - Simplified ordering table (2.1)
  - ID-Based ordering (2.1)
- DLLP Format Details
- ACK/NAK Protocol
  - Error Recovery Mechanism
  - Examples of Variety of Error Scenarios
  - Nullified Packets and Store-and Forward vs. Cut-Through Mode
- Physical Layer Logic (Gen1/Gen2)
  - Byte Striping/Unstriping
  - Scrambling/Unscambling
  - 8b/10b Encoding/Decoding
  - Serializing/Deserializing
- Physical Layer Logic (Gen3)
  - 128b/130b Encoding/Decoding
- Physical Layer Electrical (Gen1/Gen2/Gen3)
  - Differences Between Generations
  - De-emphasis
  - Gen3 Equalization
- Link Initialization & Link Training
  - Detect, Polling, Configuration, L0, Recovery (Retraining) States
  - Power Management States: L0, L0s, L1, L1 Active, L2, L3 Power States
  - Gen3 Equalization Training
  - Link Width and Speed Changing
- Error Detection and Handling
  - Correctable, Non-Fatal and Fatal Errors
  - **HANDS-ON ARBOR LAB**: Determine source and error reporting mechanism
- Power Management
  - Software controlled Power Management
  - Active Hardware-based Power Management
  - Optimized Buffer Flush Fill (OBFF) (2.1), Latency Tolerance Reporting (2.1) and L1 sub-states (3.1)
- Interrupt Support
  - Legacy Interrupt Handling
  - MSI Interrupt
  - MSI-X Interrupt
  - **HANDS-ON ARBOR LAB**: Investigate source of MSI interrupt and delivery
- System Resets
  - Fundamental Reset (Cold and Warm Reset), In-band Reset (Hot Reset)
  - Function Level Reset (FLR)
- Hot Plug and Power Budgeting
  - Hot Plug Controller
  - Dynamic Power Allocation (2.1)
- 2.1 and 3.1 ECN as required such as:

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- Internal error reporting
- Multi-casting
- Atomic Operations
- Resizable BARs
- Alternative Routing-ID Interpretation
- Extended Tag enable
- TLP Processing Hints
- Downstream Port Containment
- Lightweight Notification
- Process Address Space ID
- Precision Time Measurement
- Protocol Multiplexing
- Address Translation Services

Recommended Prerequisites:

A basic understanding of digital bus architectures such as PCI is highly recommended.

Course Material:

1) PCI Express Technology eBook (or hardcopy on request) by Mike Jackson and Ravi Budruk
2) Downloadable PDF version of the presentation slides
3) MindShare Arbor software tool, used for student labs in the class
4) Optional: Comprehensive PCI Express 2.0 eLearning course
5) Optional: PCI Express 2.1 and 3.0 Update eLearning course
6) Optional: Intro to PCI Express IO Virtualization eLearning course