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PCI Express 4.0 and 5.0 Update Architecture

Training

Let MindShare Bring "Advanced PCI Express 4.0 and 5.0 Update Architecture" To Life For You

MindShare's PCI Express 4.0 and 5.0 Update Architecture course assumes you understand the details of PCI Express 3.x architecture specification or have taken a MindShare PCI Express 3.1 course. With that as prerequisite, we then drill down into understanding what is new with PCIe 4.0 and 5.0 spec and how to achieve 16.0 GT/s and 32 GT/s transfer rates.

There are a large number of features and optional behaviors described in the PCIe spec. MindShare can customize the course to cover the topics that are most important for your group. Use the course outline below as a guide to request topics you want covered or removed.

You Will Learn:

- The process of transmitter equalization necessary to operate at 8 GT/s, 16.0GT/s and 32.0GT/s
- Overview of the LTSSM including the concepts important for each state and Speed Change process
- Capabilities added to Gen4 and Gen5 specifications

For SRIOV and ATS related topics, which are incorporated into the PCIe 5.0 spec, please request our 3-day IO Virtualization for Intel Platforms or IO Virtualization for ARM Platforms as these topics are **NOT** covered in this standard 5-day PCIe course. Additionally, PIPE 6.0 spec related topics are not covered but can be added upon request. Some of the ECNs listed below are covered upon request.

Who Should Attend?

This course is hardware-oriented, but is suitable for both hardware and software engineers because the configuration registers used to control the hardware are covered in detail. The course is ideal for RTL-, chip-, system- or system board-level design engineers who need a broad understanding of PCI Express. Given the in-depth architecture and design details covered, the course is also suitable for chip-level and board-level validation engineers.

Course Length: 1 Day (but customizable to longer duration)

Course Outline:

	Hands-On 5-day Class	PCIe Gen4/5 1-day Class
PCI Architecture Background Foundation		
PCI concepts important for understanding PCI Express	X	
Physical Address Spaces	X	
Traffic Types (System Memory, PIO and DMA)	X	
Typical System Transactions (NVMe Example)	X	

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	Hands-On 5-day Class	PCIe Gen4/5 1-day Class
PCI Express Features and Architecture Overview		
Layered Architecture	X	
ARM example topology	X	
TLP, DLLP and Ordered Set Packet Format Overview	X	
Protocol Overview	X	
Configuration Overview		
Legacy and Enhanced Configuration Access Mechanism (ECAM)	X	
Type 0 and Type 1 Headers, Capability and Extended Capability Structures	X	
Bus Enumeration	X	
HANDS-ON ARBOR LAB: Scan your system and determine topology	X	
Address Space and Transaction Routing		
Clarification of Memory space	X	
System memory vs MMIO	X	
Prefetchable vs Non-prefetchable	X	
IO space	X	
Setting up the BARs as well as the Base and Limit registers	X	
Switch Routing Mechanism	X	
HANDS-ON ARBOR LAB: Debug problem with address mapping	X	
TLP Format Details		
Normal TLP fields	X	
TLP Prefixes	X	
Lightweight Notification and TPH / Steering Tags	X	
10-bit Tags	X	X
PCI-SIG Vendor-Defined Messages	X	
Quality of Service and Arbitration		
TC/VC Mapping	X	
VC Arbitration	X	
Port Arbitration	X	
Multi-function Arbitration	X	
Flow Control		
Flow Control Protocol	X	
Scaled Flow Control	X	X
Link Feature Exchange	X	X
Flow Control Initialization	X	
Runtime Flow Control Update Mechanism	X	

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	Hands-On 5-day Class	PCIe Gen4/5 1-day Class
Transaction Ordering		
Simplified Ordering Table	X	
Relaxed and ID-Based Ordering	X	
DLLP Format Details		
DLLPs	X	
NOP & Data Link Feature DLLPs	X	X
ACK / NAK Protocol		
TLP Error Recovery Mechanism	X	
Simplified Replay Timer	X	X
Examples of Numerous Error Scenarios	X	
Nullified Packets and Cut-Through Mode Switches	X	
Physical Layer Logic (2.5GT/s and 5.0GT/s)		
Block Diagram	X	
Ordered Sets	X	
Byte Striping/Unstriping	X	
Scrambling/Unscambling	X	
8b/10b Encoding/Decoding	X	
Serializing/Deserializing	X	
Physical Layer Logic (8.0GT/s, 16.0GT/s and 32.0GT/s)		
128b/130b Encoding/Decoding	X	
Control SKPs	X	X
Ordered-Set Blocks and Data Blocks	X	
Data Streams and Packet Framing	X	
Data Parity Checking	X	X
16.0 & 32.0 GT/s Data Parity Checking	X	X
Precoding	X	X
Physical Layer Electrical (all speeds)		
Differential Tx / Rx	X	
2.5GT/s and 5.0GT/s De-emphasis	X	
8.0GT/s, 16.0GT/s and 32.0GT/s Equalization Concept	X	X
Rx Equalization	X	X
Electrical Conditions for different Link States	X	X
Spread Spectrum Clocking (SSC)	X	
Separate Refclk Independent SSC (SRIS)	X	

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	Hands-On 5-day Class	PCIe Gen4/5 1-day Class
Link Initialization and Training (LTSSM)		
Detect, Polling, Configuration, L0 States	X	X
Recovery: Link Speed Change	X	X
Recovery: Equalization Process	X	X
16.0 GT/s Equalization and Config Structures	X	X
Negotiation for skipping parts or all of Tx Equalization	X	X
32.0 GT/s Equalization and Config Structures	X	X
Recovery: Link Width Change		
L0s, L1, L2, Hot Reset, Link Disable and Loopback States	X	
Modified TS1 / TS2s and Alternate Protocol Negotiation	X	X
Interrupt Support		
Legacy Interrupt Handling		
MSI Interrupts	X	
32-bit MSI Data	X	
MSI-X Interrupts	X	
HANDS-ON ARBOR LAB: Investigate source of MSI(-X) interrupt and delivery	X	
Error Detection and Handling		
Correctable, Non-Fatal and Fatal Errors	X	
Advisory Non-Fatal Errors	X	
Error Subclass field for Correctable Error Messages		
Advanced Error Reporting (AER)	X	
HANDS-ON ARBOR LAB: Determine source and error reporting mechanism	X	
Power Management		
Device Power States	X	
Link Power States	X	
L1 Substates	X	
Link Activation		X
Active State Power Management (ASPM) - hardware controlled	X	
Software Controlled Power Management	X	
Power Management Events (PME, Beacon and #WAKE)	X	
Dynamic Power Allocation (DPA)		
Optimized Buffer Flush Fill (OBFF)		
Latency Tolerance Reporting (LTR)	X	
System Resets		
Conventional Reset Mechanisms: Cold, Warm and Hot Reset	X	
Function Level Reset (FLR)	X	

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	Hands-On 5-day Class	PCIe Gen4/5 1-day Class
Features Introduced with PCIe 4.0		
Retimers	overview	X
Lane Margining	overview	X
Flattening Portal Bridge (FPB)	overview	X
Hierarchy ID Reporting		X
Designated Vendor-Specific Extended Capability (DVSEC)	overview	X
Enhanced Allocation		X
Emergency Power Reduction State		X
Features Introduced with PCIe 5.0		
System Firmware Intermediary Support	overview	X
Other PCIe Features (ECNs)		
Hot Plug		
Power Budgeting		
Multi-Casting		
Protocol Multiplexing (PMUX)		
Resizable BARs		
Downstream Port Containment (DPC) and Enhanced DPC (eDPC)		
Lightweight Notification (can be used for lightweight cache coherency)		
Process Address Space ID (PASID)		
Precision Time Measurement (PTM)		
Device Readiness Status (DRS) and Function Readiness Status (FRS)		

Recommended Prerequisites:

An in-depth understanding of PCIe specification up to Rev 3.x or taken MindShare's PCI Express 3.x course.

Course Material:

1) PCI Express Technology eBook (or hardcopy on request) by Mike Jackson and Ravi Budruk
2) Downloadable PDF version of the presentation slides
3) Add-On Advanced PCI Express 3.x, 4.0 and 5.0 eLearning course (discounted pricing applies)