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# PCI Express 6.0 Update

## Training

### Let MindShare Bring "PCI Express 6.0 Update" to Life for You

The PCI Express (PCIe) architecture is a high-performance I/O bus used to interconnect peripheral devices in computing and communication platforms. PCIe has been around for over two decades and has evolved with the needs of the computing industry. This sixth generation of PCIe brings with it another doubling of bandwidth along with some significant changes and new features to the protocol.

This MindShare course assumes prior knowledge of PCIe 5.0. This course provides a detailed description of the new data rate of 64GT/s and PAM-4 encoding along with coverage of all the new protocol features and changes.

### **Course Length**: 2 Days

### **Course Outline**:

- 64GT/s using PAM4 signaling and 1b/1b encoding
  - Precoding and Gray Coding also used
- Introduction of fixed-sized FLITs (256 bytes each)
- FEC (Forward Error Correction) needed (lightweight for low-latency)
  - LCRCs are still used, but retry mechanism is on a FLIT basis
    - Can retry all FLITs after a bad received FLIT or only the bad FLIT(s)
  - ACKs / NAKs are per FLIT in Flit Mode
- Operating in Flit Mode (FM) vs Non-Flit Mode (NFM)
- In FM:
  - New TLP format (local prefix(es), TLP Header Base, Orthogonal Header Count (OHC), payload, TLP trailer, end-to-end suffix(es))
  - TLPs and DLLPs packed into Flits
  - Switches / Root Complexes may need to translate traffic from FM to NFM and vice-versa
  - Adding Segment info to packets for routing TLPs across different segments
  - 14-bit Tag field in TLPs
  - Flow Control can now provide both dedicated buffers as well as shared buffers across VCs
    - Also, option for merging Posted and Completion credits ("Merged" FC)
- Shadow Functions vs Phantom Functions
- Optimized Update Flow Control advertisement
- New Link Features (e.g., Immediate Readiness advertisement, L0p support, extended VC count)
- L0p link power state (sub-state of L0)
- Link Management DLLPs
- Changes to Ordered Set formats (e.g., TS1 / TS2 changes) as well as new TS0 (Training Sequence 0)
- Link Training and Tx Equalization for 64GT/s
- 64GT/s Extended Capability Structure
- FLIT Logging Extended Capability Structure
- FLIT Performance Measurement Extended Capability Structure
- FLIT Error Injection Extended Capability Structure

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- Device 3 Extended Capability Structure
- Shadow Functions Extended Capability Structure
- Power Budgeting new features

## Required Prerequisites:

Deep understanding of PCIe 5.0.

## Course Material:

1) Downloadable PDF version of the presentation slides
2) Optional: Comprehensive PCIe 5.0 eLearning course
3) Optional: PCIe 6.0. Update eLearning (when available)