

## PCI Express 6.0 Architecture

### Training

#### Let MindShare Bring “PCI Express 6.0 Architecture” To Life For You

MindShare's PCI Express System Architecture course starts with a high-level view of the technology to provide the big-picture context and then drills down into the details for each topic, providing a thorough understanding of the hardware and software protocols.

The course describes additional features added to the architecture when moving through the PCIe specification revisions from 1.1 all the way to the latest 6.0. There are a large number of features and optional behaviors described in the PCIe spec. MindShare can customize the course to cover the topics that are most important for your group. Use the course outline below as a guide to request topics you want covered or removed.

#### You Will Learn:

- PCI Express features and capabilities
- The definition and responsibilities of each of the layers in the interface
- Details of the PCIe packet-based transaction protocol
- The error detection, reporting and possible correction mechanisms
- The address space and packet-routing methods used
- How the various power management techniques work
- The details of the configuration registers that provide control and status visibility to software
- Software enumeration process
- The process of transmitter equalization necessary to operate at 8.0GT/s – 64.0GT/s
- The details of the LTSSM including the concepts important for each state
- PAM4 signaling
- Flit Mode behavior

For SRIOV and ATS related topics, which are incorporated into the PCIe base spec, please request our 3-day [IO Virtualization for Intel Platforms](#) or [IO Virtualization for ARM Platforms](#) as these topics are **NOT** covered in this standard 5-day PCIe course. Additionally, PIPE 6.0 spec related topics are not covered but can be added upon request. We can cover optional features listed below on request.

#### Who Should Attend?

This course is hardware-oriented but is suitable for both hardware and software engineers because the configuration registers used to control the hardware are covered in detail. The course is ideal for RTL-, chip-, system- or system board-level design engineers who need a broad understanding of PCI Express. Given the in-depth architecture and design details covered, the course is also suitable for chip-level and board-level validation engineers.

**Course Length:** 5 Days (but customizable to shorter duration)

**Course Outline:**

Topic	5-day Class
	PCIe 6.0
<b>PCI Architecture Background Foundation</b>	
PCI concepts important for understanding PCI Express	pre-class eLearning
Physical Address Spaces	
Traffic Types (System Memory, PIO and DMA)	
Typical System Transactions (NVMe Example)	
<b>PCI Express Features and Architecture Overview</b>	
Layered Architecture	pre-class eLearning
ARM example topology	
TLP, DLLP and Ordered Set Packet Format Overview	
Protocol Overview	
<b>Configuration Overview</b>	
Legacy and Enhanced Configuration Access Mechanism (ECAM)	pre-class eLearning
Type 0 and Type 1 Headers, Capability and Extended Capability Structures	
Bus Enumeration	
<b>HANDS-ON ARBOR LAB:</b> Scan your system and determine topology	
<b>Address Space and Transaction Routing</b>	
Clarification of Memory space	pre-class eLearning
System memory vs MMIO	
Prefetchable vs Non-prefetchable	
IO space	
Setting up the BARs as well as the Base and Limit registers	
Switch Routing Mechanism	
<b>HANDS-ON ARBOR LAB:</b> Debug problem with address mapping	
<b>TLP Format Details</b>	
Normal TLP fields	X
TLP Prefixes	X
10-bit Tags	X
PCI-SIG Vendor-Defined Messages	X
<b>Quality of Service and Arbitration</b>	
TC/VC Mapping	
VC Arbitration	
Port Arbitration	
Multi-function Arbitration	
<b>Flow Control</b>	
Flow Control Protocol	X
Scaled Flow Control	X
Link Feature Exchange	X
Flow Control Initialization	X
Runtime Flow Control Update Mechanism	X
<b>Transaction Ordering</b>	
Simplified Ordering Table	overview
Relaxed and ID-Based Ordering	overview
<b>DLLP Format Details</b>	
DLLPs	X
NOP & Data Link Feature DLLPs	X
<b>ACK / NAK Protocol</b>	
TLP Error Recovery Mechanism	X

Simplified Replay Timer	X
Examples of Numerous Error Scenarios	X
Nullified Packets and Cut-Through Mode Switches	X
<b>Physical Layer Logic (2.5GT/s and 5.0GT/s)</b>	
Block Diagram	X
Ordered Sets	X
Byte Striping/Unstriping	X
Scrambling/Unscrambling	X
8b/10b Encoding/Decoding	X
Serializing/Deserializing	X
<b>Physical Layer Logic (8.0GT/s, 16.0GT/s and 32.0GT/s)</b>	
128b/130b Encoding/Decoding	X
Control SKPs	X
Ordered-Set Blocks and Data Blocks	X
Data Streams and Packet Framing	X
Data Parity Checking	
16.0 & 32.0 GT/s Data Parity Checking	
Precoding	X
<b>Physical Layer Electrical (all speeds)</b>	
Differential Tx / Rx	X
2.5GT/s and 5.0GT/s De-emphasis	X
8.0GT/s, 16.0GT/s and 32.0GT/s Equalization Concept	X
Rx Equalization	overview
Electrical Conditions for different Link States	
Spread Spectrum Clocking (SSC)	overview
Separate Refclk Independent SSC (SRIS)	overview
<b>Link Initialization and Training (LTSSM)</b>	
Detect, Polling, Configuration, L0 States	X
Recovery: Link Speed Change	X
Recovery: Equalization Process	X
16.0 GT/s Equalization and Config Structures	X
Negotiation for skipping parts or all of Tx Equalization	X
32.0 GT/s Equalization and Config Structures	X
Recovery: Link Width Change	
L0s, L1, L2, Hot Reset, Link Disable and Loopback States	
Modified TS1 / TS2s and Alternate Protocol Negotiation	
<b>Interrupt Support</b>	
Legacy Interrupt Handling	
MSI Interrupts	
32-bit MSI Data	
MSI-X Interrupts	
<b>HANDS-ON ARBOR LAB:</b> Investigate source of MSI(-X) interrupt and delivery	
<b>Error Detection and Handling</b>	
Correctable, Non-Fatal and Fatal Errors	X
Advisory Non-Fatal Errors	X
Error Subclass field for Correctable Error Messages	
Advanced Error Reporting (AER)	X
<b>HANDS-ON ARBOR LAB:</b> Determine source and error reporting mechanism	
<b>Power Management</b>	
Device Power States	
Link Power States	
L1 Substates	

Active State Power Management (ASPM) - hardware controlled	
Software Controlled Power Management	
Power Management Events (PME, Beacon and #WAKE)	
Dynamic Power Allocation (DPA)	
Optimized Buffer Flush Fill (OBBF)	
Latency Tolerance Reporting (LTR)	
<b>System Resets</b>	
Conventional Reset Mechanisms: Cold, Warm and Hot Reset	X
Function Level Reset (FLR)	X
<b>1b/1b Physical Layer (PCIe 6.0)</b>	
PAM4	X
Precoding, Gray Coding and Forward Error Correction (FEC)	X
LTSSM Updates (TS0s, Tx EQ changes, entering Flit Mode, etc.)	X
<b>Flit Mode</b>	
Flit Format	X
Error Correction and Flit Retry (Standard vs Selective)	X
DLP Bytes in Flit and Flit Types	X
Flow Control (Dedicated vs Shared)	X
TLP Structure (Header Base, OHC, TLP Trailer, etc.)	X
Segments	X
L0p	X
<b>Miscellaneous PCIe Features</b>	
Retimers (introduced in 4.0)	overview
Lane Margining (introduced in 4.0)	
Flattening Portal Bridge (FPB) (introduced in 4.0)	
Hierarchy ID Reporting (introduced in 4.0)	
Designated Vendor-Specific Extended Capability (DVSEC) (introduced in 4.0)	
Enhanced Allocation (introduced in 4.0)	
Emergency Power Reduction State (introduced in 4.0)	
System Firmware Intermediary Support (introduced in 5.0)	
Hot Plug	
Power Budgeting	
Multi-Casting	
Protocol Multiplexing (PMUX)	
Resizable BARs	
Downstream Port Containment (DPC) and Enhanced DPC (eDPC)	
Lightweight Notification (can be used for lightweight cache coherency)	
Process Address Space ID (PASID)	
Precision Time Measurement (PTM)	
Device Readiness Status (DRS) and Function Readiness Status (FRS)	

### Recommended Prerequisites:

A basic understanding of digital bus architectures such as PCI is recommended.

### Course Material:

- 1) [PCI Express Technology eBook](#) (or hardcopy on request) by Mike Jackson and Ravi Budruk
- 2) Downloadable PDF version of the presentation slides
- 3) [Fundamentals of PCI Express](#) (needed for pre-work before class)
- 4) Add-On [Comprehensive PCI Express eLearning course](#) (discounted pricing applies)
- 5) Add-On PCI Express 6.0 Update eLearning Course (when released; discounted pricing applies)
- 6) Add-On MindShare [Arbor software tool](#), used for student labs in the class (discounted pricing applies)