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PCI Express 6.0 Update

Training

Let MindShare Bring "PCI Express 6.0 Update" To Life For You

MindShare's PCI Express 6.0 Update course starts with a discussion of what's new in the 6.0 spec and why the introduction of PAM4 signaling caused the need for Flits and forward error correction.

This MindShare course requires prior knowledge of PCIe 5.0. Only the new features of 6.0 are covered with a light review of 5.0 features/behaviors that have changed moving into 6.0 with Flit Mode.

You Will Learn:

- PAM4 signaling
- The need for Forward Error Correction
- Behavior of the Physical Layer at 64GT/s
- Flit format
- Ack/Nak protocol at the Flit level
- Shared vs Dedicated Flow Control Buffers
- TLP Format while in Flit Mode
- The need for Segments in some TLPs
- Benefits and operation of L0p

Who Should Attend?

This course is for anyone who has a solid understanding of PCIe 5.0 and would like to quickly get up-to-speed on PCIe 6.0.

Course Length: 3 Days

Course Outline:

Topic	3-day Class PCIe 6.0 Update
PCI Architecture Background Foundation	
PCI concepts important for understanding PCI Express	
Physical Address Spaces	
Traffic Types (System Memory, PIO and DMA)	
Typical System Transactions (NVMe Example)	
PCI Express Features and Architecture Overview	
Layered Architecture	
ARM example topology	
TLP, DLLP and Ordered Set Packet Format Overview	
Protocol Overview	
Configuration Overview	
Legacy and Enhanced Configuration Access Mechanism (ECAM)	
Type 0 and Type 1 Headers, Capability and Extended Capability Structures	
Bus Enumeration	refresher
HANDS-ON ARBOR LAB: Scan your system and determine topology	
Address Space and Transaction Routing	
Clarification of Memory space	

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System memory vs MMIO	
Prefetchable vs Non-prefetchable	
IO space	
Setting up the BARs as well as the Base and Limit registers	
Switch Routing Mechanism	
HANDS-ON ARBOR LAB: Debug problem with address mapping	

TLP Format Details

Normal TLP fields	refresher
TLP Prefixes	
10-bit Tags	
PCI-SIG Vendor-Defined Messages	

Quality of Service and Arbitration

TC/VC Mapping	
VC Arbitration	
Port Arbitration	
Multi-function Arbitration	

Flow Control

Flow Control Protocol	refresher
Scaled Flow Control	
Link Feature Exchange	
Flow Control Initialization	
Runtime Flow Control Update Mechanism	

Transaction Ordering

Simplified Ordering Table	
Relaxed and ID-Based Ordering	

DLLP Format Details

DLLPs	
NOP & Data Link Feature DLLPs	refresher

ACK / NAK Protocol

TLP Error Recovery Mechanism	refresher
Simplified Replay Timer	
Examples of Numerous Error Scenarios	
Nullified Packets and Cut-Through Mode Switches	

Physical Layer Logic (2.5GT/s and 5.0GT/s)

Block Diagram	
Ordered Sets	refresher
Byte Striping/Unstriping	
Scrambling/Unscambling	
8b/10b Encoding/Decoding	
Serializing/Deserializing	

Physical Layer Logic (8.0GT/s, 16.0GT/s and 32.0GT/s)

128b/130b Encoding/Decoding	
Control SKPs	
Ordered-Set Blocks and Data Blocks	
Data Streams and Packet Framing	
Data Parity Checking	
16.0 & 32.0 GT/s Data Parity Checking	
Precoding	

Physical Layer Electrical (all speeds)

Differential Tx / Rx	
2.5GT/s and 5.0GT/s De-emphasis	
8.0GT/s, 16.0GT/s and 32.0GT/s Equalization Concept	refresher

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Rx Equalization	
Electrical Conditions for different Link States	
Spread Spectrum Clocking (SSC)	
Separate Refclk Independent SSC (SRIS)	

Link Initialization and Training (LTSSM)

Detect, Polling, Configuration, L0 States	refresher
Recovery: Link Speed Change	
Recovery: Equalization Process	
16.0 GT/s Equalization and Config Structures	
Negotiation for skipping parts or all of Tx Equalization	
32.0 GT/s Equalization and Config Structures	
Recovery: Link Width Change	
L0s, L1, L2, Hot Reset, Link Disable and Loopback States	
Modified TS1 / TS2s and Alternate Protocol Negotiation	

Interrupt Support

Legacy Interrupt Handling	
MSI Interrupts	
32-bit MSI Data	
MSI-X Interrupts	
HANDS-ON ARBOR LAB: Investigate source of MSI(-X) interrupt and delivery	

Error Detection and Handling

Correctable, Non-Fatal and Fatal Errors	
Advisory Non-Fatal Errors	
Error Subclass field for Correctable Error Messages	
Advanced Error Reporting (AER)	
HANDS-ON ARBOR LAB: Determine source and error reporting mechanism	

Power Management

Device Power States	
Link Power States	
L1 Substates	
Active State Power Management (ASPM) - hardware controlled	
Software Controlled Power Management	
Power Management Events (PME, Beacon and #WAKE)	
Dynamic Power Allocation (DPA)	
Optimized Buffer Flush Fill (OBFF)	
Latency Tolerance Reporting (LTR)	

System Resets

Conventional Reset Mechanisms: Cold, Warm and Hot Reset	
Function Level Reset (FLR)	

1b/1b Physical Layer (PCIe 6.0)

PAM4	X
Precoding, Gray Coding and Forward Error Correction (FEC)	X
LTSSM Updates (TS0s, Tx EQ changes, entering Flit Mode, etc.)	X

Flit Mode

Flit Format	X
Error Correction and Flit Retry (Standard vs Selective)	X
DLP Bytes in Flit and Flit Types	X
Flow Control (Dedicated vs Shared)	X
TLP Structure (Header Base, OHC, TLP Trailer, etc.)	X
Segments	X
L0p	X

Miscellaneous PCIe Features

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Retimers (introduced in 4.0)	
Lane Margining (introduced in 4.0)	
Flattening Portal Bridge (FPB) (introduced in 4.0)	
Hierarchy ID Reporting (introduced in 4.0)	
Designated Vendor-Specific Extended Capability (DVSEC) (introduced in 4.0)	
Enhanced Allocation (introduced in 4.0)	
Emergency Power Reduction State (introduced in 4.0)	
System Firmware Intermediary Support (introduced in 5.0)	
Hot Plug	
Power Budgeting	
Multi-Casting	
Protocol Multiplexing (PMUX)	
Resizable BARs	
Downstream Port Containment (DPC) and Enhanced DPC (eDPC)	
Lightweight Notification (can be used for lightweight cache coherency)	
Process Address Space ID (PASID)	
Precision Time Measurement (PTM)	
Device Readiness Status (DRS) and Function Readiness Status (FRS)	

Required Prerequisites:

A good understanding of PCIe 5.0.

Course Material:

1) PCI Express Technology eBook (or hardcopy on request) by Mike Jackson and Ravi Budruk
2) Downloadable PDF version of the presentation slides
3) Add-On PCI Express 6.0 Update eLearning course (when released; discounted pricing applies)
4) Add-On Comprehensive PCI Express eLearning course (discounted pricing applies)