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PCI Express Architecture Fundamentals

Training

Let MindShare Bring "PCI Express Architecture Fundamentals" To Life For You

The PCI Express (PCIe) architecture is high-performance I/O bus used to interconnect peripheral devices in computing and communication platforms.

MindShare's PCI Express System Architecture Fundamentals course starts with a high-level view of the PCIe protocol to provide the big-picture context and then provides an overview of each part of the design such as interrupt handling, error handling and power management. We also provide an overview of features added in each generation of the PCIe spec revision 1.1 to 2.0 to 3.0 to 4.0 and to 5.0.

Each new generation of PCIe doubles the bandwidth compared to the previous generation. This short 'Fundamentals' course provides a high-level understanding of the protocol and how bandwidth doubling is achieved with each new generation of PCIe. There are a large number of features and optional behaviors described in the PCIe spec. MindShare can customize the course to cover the topics that are most important for your group. Use the course outline below as a guide to request topics you want covered or removed.

You Will Learn:

- PCI Express features and capabilities of Gen1 to Gen5
- The definition and responsibilities of each of the layers in the interface
- Overview of packet-based protocol used by PCIe
- The important configuration registers that provide control and status visibility to software
- MSI Interrupt handling, error handling, power management overview

Who Should Attend?

This course is suitable for Hardware/Software/Firmware engineers or management looking to get a broad understanding of PCIe protocol.

Course Length: 1 Day

Course Outline:

	Hands-On 5-day Class	Fundamentals 1-day Class
PCI Architecture Background Foundation		
PCI concepts important for understanding PCI Express	X	
Physical Address Spaces	X	X
Traffic Types (System Memory, PIO and DMA)	X	X
Typical System Transactions (NVMe Example)	X	X

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	Hands-On 5-day Class	Fundamentals 1-day Class
PCI Express Features and Architecture Overview		
Layered Architecture	X	X
ARM example topology	X	X
TLP, DLLP and Ordered Set Packet Format Overview	X	X
Protocol Overview	X	X
Configuration Overview		
Legacy and Enhanced Configuration Access Mechanism (ECAM)	X	X
Type 0 and Type 1 Headers, Capability and Extended Capability Structures	X	X
Bus Enumeration	X	
HANDS-ON ARBOR LAB: Scan your system and determine topology	X	
Address Space and Transaction Routing		
Clarification of Memory space	X	X
System memory vs MMIO	X	X
Prefetchable vs Non-prefetchable	X	
IO space	X	
Setting up the BARs as well as the Base and Limit registers	X	
Switch Routing Mechanism	X	
HANDS-ON ARBOR LAB: Debug problem with address mapping	X	
TLP Format Details		
Normal TLP fields	X	
TLP Prefixes	X	
Lightweight Notification and TPH / Steering Tags	X	
10-bit Tags	X	
PCI-SIG Vendor-Defined Messages	X	
Quality of Service and Arbitration		
TC/VC Mapping	X	
VC Arbitration	X	
Port Arbitration	X	
Multi-function Arbitration	X	
Flow Control		
Flow Control Protocol	X	
Scaled Flow Control	X	
Link Feature Exchange	X	
Flow Control Initialization	X	
Runtime Flow Control Update Mechanism	X	

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Transaction Ordering		
Simplified Ordering Table	X	
Relaxed and ID-Based Ordering	X	
DLLP Format Details		
DLLPs	X	
NOP & Data Link Feature DLLPs	X	
ACK / NAK Protocol		
TLP Error Recovery Mechanism	X	
Simplified Replay Timer	X	
Examples of Numerous Error Scenarios	X	
Nullified Packets and Cut-Through Mode Switches	X	
Physical Layer Logic (2.5GT/s and 5.0GT/s)		
Block Diagram	X	
Ordered Sets	X	
Byte Striping/Unstriping	X	
Scrambling/Unscambling	X	
8b/10b Encoding/Decoding	X	
Serializing/Deserializing	X	
Physical Layer Logic (8.0GT/s, 16.0GT/s and 32.0GT/s)		
128b/130b Encoding/Decoding	X	
Control SKPs	X	
Ordered-Set Blocks and Data Blocks	X	
Data Streams and Packet Framing	X	
Data Parity Checking	X	
16.0 & 32.0 GT/s Data Parity Checking	X	
Precoding	X	
Physical Layer Electrical (all speeds)		
Differential Tx / Rx	X	
2.5GT/s and 5.0GT/s De-emphasis	X	
8.0GT/s, 16.0GT/s and 32.0GT/s Equalization Concept	X	
Rx Equalization	X	
Electrical Conditions for different Link States	X	
Spread Spectrum Clocking (SSC)	X	
Separate Refclk Independent SSC (SRIS)	X	

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Link Initialization and Training (LTSSM)		
Detect, Polling, Configuration, L0 States	X	overview
Recovery: Link Speed Change	X	
Recovery: Equalization Process	X	
16.0 GT/s Equalization and Config Structures	X	
Negotiation for skipping parts or all of Tx Equalization	X	
32.0 GT/s Equalization and Config Structures	X	
Recovery: Link Width Change		
L0s, L1, L2, Hot Reset, Link Disable and Loopback States	X	
Modified TS1 / TS2s and Alternate Protocol Negotiation	X	
Interrupt Support		
Legacy Interrupt Handling		
MSI Interrupts	X	overview
32-bit MSI Data	X	
MSI-X Interrupts	X	
HANDS-ON ARBOR LAB: Investigate source of MSI(-X) interrupt and delivery	X	
Error Detection and Handling		
Correctable, Non-Fatal and Fatal Errors	X	overview
Advisory Non-Fatal Errors	X	
Error Subclass field for Correctable Error Messages		
Advanced Error Reporting (AER)	X	
HANDS-ON ARBOR LAB: Determine source and error reporting mechanism	X	
Power Management		
Device Power States	X	
Link Power States	X	
L1 Substates	X	
Link Activation		
Active State Power Management (ASPM) - hardware controlled	X	
Software Controlled Power Management	X	
Power Management Events (PME, Beacon and #WAKE)	X	
Dynamic Power Allocation (DPA)		
Optimized Buffer Flush Fill (OBFF)		
Latency Tolerance Reporting (LTR)	X	
System Resets		
Conventional Reset Mechanisms: Cold, Warm and Hot Reset	X	
Function Level Reset (FLR)	X	

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	Hands-On 5-day Class	Fundamentals 1-day Class
Features Introduced with PCIe 4.0		
Retimers	overview	overview
Lane Margining	overview	overview
Flattening Portal Bridge (FPB)	overview	
Hierarchy ID Reporting		
Designated Vendor-Specific Extended Capability (DVSEC)	overview	
Enhanced Allocation		
Emergency Power Reduction State		
Features Introduced with PCIe 5.0		
System Firmware Intermediary Support	overview	overview
Other PCIe Features (ECNs)		
Hot Plug		
Power Budgeting		
Multi-Casting		
Protocol Multiplexing (PMUX)		
Resizable BARs		
Downstream Port Containment (DPC) and Enhanced DPC (eDPC)		
Lightweight Notification (can be used for lightweight cache coherency)		
Process Address Space ID (PASID)		
Precision Time Measurement (PTM)		
Device Readiness Status (DRS) and Function Readiness Status (FRS)		

Recommended Prerequisites:

A basic understanding of digital bus architectures such as PCI is highly recommended.

Course Material:

1) PCI Express Technology eBook (or hardcopy on request) by Mike Jackson and Ravi Budruk
2) Downloadable PDF version of the presentation slides
3) Add-On Fundamentals of PCI Express eLearning course (discounted pricing applies)