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PIPE 6.0 – PHY Interface for PCI Express and more

Training

Let MindShare Bring "PIPE 6.0 – PHY Interface for PCI Express and more" To Life For You

This MindShare course describes the MAC/PHY interface as described in **P**HY **I**nterface for the **P**CI **E**xpress, SATA, USB , DisplayPort and USB4 Architectures 6.0 (**PIPE** 6.0) specification.

PIPE 6.0 enables the development of PHYs for PCI Express, SATA, USB, DisplayPort, and USB4. Such PIPE compliant PHYs can be delivered as standalone ICs or as macrocell IPs for inclusion in ASICs. The course describes a standard interface between such a PHY and a Media Access Layer (MAC) & Link Layer ASIC. Two independently designed PHY and MAC ASICs/macrocell IPs will connect and work together as long as they meet the design requirements of PIPE 6.0. This course does not describe the internal design of a compliant PHY chip or higher layer protocol architecture. To understand PCIe, SATA or USB architecture, you would need to take one of MindShare's other comprehensive architecture courses.

The course covers PIPE interface operational behavior in PCIe, USB and SATA modes. Additionally, you will also learn the signaling protocol associated with the Link Training process, Equalization process and Lane Margining

You Will Learn:

- Signals and protocol associated with communication between the MAC layer (of PCIe, SATA, USB 3.1, USB4 and DisplayPort) and PHY layer
- Register definitions both in the MAC and PHY layers
- Signaling to support the PHY equalization process
- PCIe power state support
- USB and SATA operational modes

Who Should Attend?

This in-depth course is for anyone looking to understand PIPE (PHY Interface for PCI Express, SATA, USB3.1, DisplayPort and USB4), its signals and how it is used for different protocols.

Course Length: 1 Day

Course Outline:

- Introduction to the PIPE Interface
- PHY/MAC Interface
- PHY Registers
- MAC Registers
- PIPE Operational Behavior: PCIe Mode
- Equalization Process
- PCIe Lane Margining
- PCIe Elastic Buffer
- PCIe Power States
- PIPE Operational Behavior: USB Mode
- PIPE Operational Behavior: SATA Mode

Recommended Prerequisites:

A basic understanding of PCI Express, SATA, USB 3.1/USB4 and DisplayPort protocols which serves as a basis to understanding the packets and signals that traverse the PIPE interface.

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Course Material:

1) PCI Express Technology eBook (or hardcopy on request) by Mike Jackson and Ravi Budruk
2) Downloadable PDF version of the presentation slides
3) Optional: PIPE 6.0 – PHY Interface for PCI Express and more eLearning course