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Serial ATA (SATA) 3.2 with AHCI Overview

Let MindShare Bring "Serial ATA (SATA) 3.2 with AHCI Overview" to Life for You
MindShare brings the SATA course to life through its interactive classroom style, demonstrations, and hands-on exercises. This course covers the SATA 3.2 specification from a hardware design perspective and also discusses the software requirements of SATA implementations (Includes SATA Express and M.2). The Advanced Host Controller Interface (AHCI) is also described along with its numerous registers.

You Will Learn:

- The sequence of events associated with SATA initialization, including Out Of Band (OOB) signaling
- Detailed operation of a SATA HBA and drive when executing legacy commands
- How to verify proper command protocol associated with each of the command categories
- How to verify proper control protocol associated with writes to the Control register
- How to validate proper FIS (Frame Information Structure) protocol given trace captures from a SATA protocol analyzer
- The actions taken by each layer in the SATA interface
- The details associated with the implementation of Port Multipliers
- The operation and performance advantages of Native Command Queuing (NCQ)
- SATA Express implementation and features
- M.2 sockets and modules for SSD applications
- Advanced Host Controller Interface (AHCI) Overview
- How to use Arbor to view AHCI registers

Course Length: 3 Days

Who Should Attend?
Hardware designers, software developers, and system validation engineers will all benefit from this course. Both hardware and software requirements of a SATA subsystem are detailed and explained through numerous examples and the use of protocol analyzer traces.

Course Contents:

- Part I: SATA Overview
  - Evolution of Parallel ATA
  - Motivation for SATA
  - SATA Overview
  - **ARBOR LAB:** Scan system and understand Arbor features
- Part II: FIS Transmission Protocols
  - FIS Types & Formats
  - Transport & Link Protocol Details
  - FIS Retry (Transport Layer)
  - Data Flow Control
  - Physical Layer Functions
  - Error Detection & Handling
- Part III: Command & Control Protocols
  - Device Control Protocols
  - Device Command Protocols
  - Native Command Queuing (NCQ)
  - NCQ Protocols

- New Commands & Subcommands
- NCQ Log Addresses
- **ARBOR LAB:** Verify NCQ operation

- Part IV: Server Implementations
  - Port Multipliers
  - Port Selectors
  - Enclosure Services
- Part V: Physical Layer Details
  - SATA Initialization
  - AFE & Electrical Details
  - Link Power Management
  - Hot Plug
  - Built-In Test (BIST)
  - Cables/Connectors
- Part VI SATA Express (SATA-IO) Overview
  - Introduction to SATA Express
  - SATA Express Connectors / Receptacles
  - PCIe Drives/SATA Drives/SATA Legacy Drives
  - Connector Matrix
  - SATA Express Pinouts
- Part VII M.2 Sockets & Modules (PCI SIG) Overview
  - Introduction to M.2
  - Socket 2 & Socket 3 for SSDs
  - M.2 Supports SATA/PCIe Speeds
  - Module dimensions
  - M.2 Pinouts
- Part VIII: Advanced Host Controller Interface Overview
  - PCIe Configuration of AHCI
  - **ARBOR LAB:** Evaluating the AHCI Capability Registers
  - **ARBOR LAB:** Evaluating the Port Registers
  - **ARBOR LAB:** Evaluating the Memory Structures

Recommended Prerequisites:

A solid understanding of one or more storage bus protocols such as ATA or similar architecture is recommended but not required.

Course Material:

1) Presentation PDF handout
2) MindShare's SATA Storage Technology eBook (PDF)
   Author: Don Anderson
3) Optional: License to MindShare Arbor Software test and debug tool to access AHCI controller registers
4) Optional: SATA 3.2 Technology eLearning course
5) Optional: Advanced Host Controller Interface (AHCI) eLearning course