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Universal Chiplet Interconnect Express (UCIe) Architecture

Let MindShare Bring "Universal Chipset Interconnect Express (UCIe) 1.0 Architecture" to Life for You

Universal Chiplet Interconnect Express (UCIe) is an open industry standard, multi-protocol, high-bandwidth (up to 32GT/s per lane), die-to-die (chiplet), interconnect that standardizes inter-die communication on-package. The UCIe 1.0 specification enables users to mix and match chiplet components from a multi-vendor ecosystem for System-on-Chip (SoC) build. The UCIe spec describes a standardized port and interconnect with physical layer, protocol stack and software model that enables inter-chiplet communication. UCIe supports multiple protocols such as PCIe, CXL, and a raw mode that can be used to map any protocol of choice (assuming both ends support it) on top of a common Physical and Link layer. The spec describes elements needed for SoC design such as the application layer, form-factors relevant to the package including bump location, power delivery and thermal solution. The specification will evolve into future revisions but will ensure backward compatibility to the 1.0 revision.

The initial protocols being mapped to UCIe are PCIe and CXL and are done using a Flit packet format for communication. Both PCIe and CXL protocol mappings will enable more on-package integration by replacing the PCIe SERDES PHY, the PCIe/CXL Logical Physical layer and the Link Level Retry (LLR) state-machines with a UCIe Adapter and PHY in order to improve the power and performance characteristics. UCIe also supports a protocol-agnostic raw mode to enable other protocols to be mapped.

MindShare's comprehensive UCIe Architecture course provides a solid foundation to understanding die-to-die architecture and use of UCIe retimers to extend connectivity beyond the package. The course describes port architecture details including protocol layer, die-to-die adapter layer, logical physical layer and electrical physical layer. We describe single and multi-module configurations. In addition, the course describes the sideband architecture details. Sideband interface is used for back-channel Link training, access to registers, Link management packets and parameter exchanges with remote Link partner. UCIe register architecture and the mechanism by which UCIe-aware SW discovers UCIe capability is described. An optional section describes a Raw Die-to-Die Interface (RDI) and Flit-aware Die-to-Die Interface (FDI) between the die-to-die adapter layer and physical layer.

You Will Learn:

- UCIe system architecture used for die-to-die communication including use of UCIe retimers
- UCIe for tunneling PCIe, CXL and other protocols in raw mode
- UCIe port design constituting Protocol, Die-to-Die Adapter, Logical and Electrical Physical Layers
- Sideband interface usage and protocol
- Software view of UCIe when paired with PCIe or CXL protocol layers
- UCIe Interface (RDI and FDI) architecture between the Die-to-Die Adapter layer and Physical layer. This topic is optionally covered

Course Length: 3-Days or 4-Days with optional topics covered

Who Should Attend?

This course is hardware-oriented but is suitable for both hardware design and software engineers given the course covers UCIe registers and initialization topics. The course is ideal for RTL-, chip-, system- or system board-level design engineers who need a broad understanding of UCIe architecture. The course is also suitable for chip-level validation engineers.

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Course Outline:

- UCIe Features and Architecture Overview
  - Package and platform architecture based on UCIe
  - Overview of UCIe port architecture
    - Protocol layer
    - Die-to-Die Adapter layer
    - Logical and Electrical Physical layer
    - Sideband interface
  - RDI and FDI Interface overview
  - Single- and multi-module configurations
  - UCIe Retimers
  - Interoperability issues
- UCIe Protocol Layer Raw and Flit Modes
  - PCIe 6.0 mode
  - CXL 3.0 256B Flit mode
  - CXL 2.0 mode or 68B-Enhanced Flit mode
  - Other protocols streaming mode
- UCIe Die-to-Die Adapter Layer
  - Link/Adapter initialization
  - Modes of operation
    - Raw Mode for all protocols
    - CXL 2.0 or "CXL 68B-Enhanced Flit Mode"
    - PCIe 6.0 or "CXL 256B Flit Mode" with Standard 256B Flit
    - "CXL 256B Flit Mode" with Latency-Optimized 256B Flit
  - Protocol and Flit format
  - Power management link states
  - Retry rules
  - Parity-based runtime Link testing
- UCIe Logical Physical Layer
  - Data and sideband transmission flows
  - Lane reversal
  - Interconnect redundancy map
  - Data to clock training and test modes
  - Link Initialization and Training
  - Runtime recalibration
  - Multi-module Link initialization
- UCIe Electrical Physical Layer
  - Interoperability of data rates
  - Tx spec
  - Rx spec
  - Clocking
  - Supply noise and clock skew
  - Ball-out and channel spec
  - Tightly coupled mode
  - Interconnect reducancy mapping
  - BER requirements
  - Valid and clock gating
  - Electrical Idle
  - Sideband signaling
- Sideband Interface
  - Packet types and formats
  - Flow control and data integrity
  - Operation on RDI and FDI
- UCIe Registers and Initialization/Enumeration

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- Software view of UCIe
- Software discovery of UCIe Links
- Register location and access mechanisms
- UCIe registers
- UCIe Interrupt architecture

Optional Topics (Extra 1-day)

- UCIe Interfaces between Die-to-Die Adapter and Physical Layer
  - Raw Die-to-Die Interface (RDI)
  - Flit-Aware Die-to-Die Interface (FDI)
  - Rules for RDI and FDI

Recommended Prerequisites:

Good working knowledge of PCI Express (PCIe) and Compute Express Link (CXL) a must. Computer architecture fundamentals. Some knowledge of Intel, AMD or Arm processor architectures.

Course Material:

1) Downloadable PDF version of the presentation slides
2) Optional UCIe 1.0 eLearning course when available