1-512-256-0197
www.mindshare.com
training@mindshare.com

USB 3.2 Update Course

Training

Let MindShare Bring "USB 3.2 Enhancements" To Life For You

The USB 3.2 specification carries forward the dual bus topology introduced in the earlier USB 3.x specifications. The dual bus model provides for a legacy USB 2.0 interface coexisting side-by-side with a SuperSpeed interface on the same physical connection. Compliant cables, plugs, and receptacles support both sets of signals. At attachment, peripheral devices connect to a host or external hub port using only one of the interfaces. Attachment is made at the highest performance protocol/speed supported by the two link partners. Hubs connect upstream using both interfaces. If both upstream connections are successful, the hub will be prepared to handle a mix of USB devices attached to its downstream facing ports.

One of the most significant USB 3.2 enhancements is the option for *dual-lane* traffic on the Enhanced SuperSpeed (ESS) interface. Prior to USB 3.2, all generations of USB were based on single-lane serial bus communications. SuperSpeed and SuperSpeedPlus as defined in the USB 3.1 specification is a dual-simplex connection with one differential signal pair for each direction (Tx/Rx). With USB 3.2 dual-lane signaling uses two differential pairs in each direction.

Who Should Attend?

This course is designed with hardware, software, and validation engineers in mind. The assumption is that attendees have some background in USB 3.0 or USB 3.1 protocol.

Course Length: 1 Day

Agenda:

- USB 3.2 Topology Overview
  - Type-C signals enable dual lane connections
  - The dual-bus topology
  - Seven connection options and bandwidth comparison
  - ESS connection priority and fallback
- USB 3.2 Hub Requirements
  - Two hub modes: SuperSpeed and SuperSpeedPlus
  - Upstream attachment impact on downstream protocols
  - Bus-powered and self-powered hubs
  - Downstream VBUS power: unit load based, USB-C based, USB Power Delivery based
- USB 3.2 Protocol and Link Layer Changes
  - Protocol Layer: Isochronous service changes
  - Link Layer: Gen 2x2 HP Buffers & Credits, Pending_HP_Timer and re-timers
- USB 3.2 Physical Layer
  - Signals
  - Gen 1x2 Tx PHY and byte striping
  - Gen 1x2 Rx PHY and byte un-striping
  - Gen 2x2 Tx PHY and byte striping
  - Gen 2x2 Rx PHY and byte un-striping
- USB 3.2 Link Training
  - SS and SSP operational modes
  - Configuration lane
  - Gen 2x2 link training example
  - Impact of re-timers
  - Initial Header Seq# and flow control credit advertisements
  - Port Configuration LMP changes

1-800-633-1440
www.mindshare.com
training@mindshare.com

Recommended Prerequisites: Background in USB 3.0 or USB 3.1 protocol.

Course materials:

Students will be provided with:

1. An electronic (PDF) version of the presentation used in class