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USB 3.1 Fundamentals

Training

Let MindShare "USB 3.1 Fundamentals" to Life for You

The Universal Serial Bus (USB) has been in existence for almost 20 years and is the most widely used IO interface in the world. Starting with USB 1.0, each new generation of this plug-and-play bus has added enhancements while remaining backward compatible with its predecessors. With the release of revision USB 3.1, features now include five possible transfer speeds referred to as Low Speed, Full Speed, High Speed, SuperSpeed (Gen 1), and SuperSpeedPlus (Gen 2). Most devices, hubs, and host controllers support multiple speeds, but always observe the defined set of protocol rules for the current operating speed. An important distinction is made between the lower three speeds (Low, Full, High Speed) and the two higher speeds (SuperSpeed and SuperSpeedPlus). In a USB 3.1 topology, two independent sets of signals are used: one signal set handles interfaces operating at Low, Full, or High Speed (also referred to as a legacy USB 2.0 rate); the other set of signals handles interfaces operating at SuperSpeed or SuperSpeedPlus (also referred to as an Enhanced SuperSpeed rate). Because any mix of USB 2.0 and Enhanced SuperSpeed devices may co-exist in a USB 3.1 system, the tasks of evaluating performance and interactions between software, USB topology, and other platform resources requires a basic understanding of the topics introduced in this course.

Who Should Attend?

This one-day course targets engineering and marketing managers, FAEs, FSEs, and others requiring a high-level understanding of the key attributes of a USB 3.1 system, including the features and limitations of each generation of USB devices and hubs. MindShare also offers additional comprehensive training courses covering details of USB protocol as well Intel's eXtensible Host Controller Interface (xHCI)

Course Length: 1 Day

Course Outline:

- USB 3.1 System Topology: The Big Picture
  - USB 2.0 Elements
    - USB 2.0 Host Controller Logic
    - USB 2.0 Low, Full, High Speed Devices and Hubs
  - Enhanced SuperSpeed Elements
    - USB 3.1 Enhanced SuperSpeed Host Controller Logic
    - USB 3.0 Devices and Hubs
    - USB 3.1 Devices and Hubs
- USB 2.0 Background
  - Original USB Motivations
  - USB 2.0 Topologies
    - Host Controller Logic
    - Hubs
    - Devices
    - 2.0 Cables and Connectors
  - Device Requests
  - USB 2.0 Packet Protocol
    - Broadcast Transactions
    - Token-Data-Handshake Model
    - IN and OUT Transaction Examples
    - Maximum Payload Sizes
  - USB 2.0 Transaction Generation and Scheduling

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- USB 2.0 Device VBus Power
- USB 3.0 Overview
  - USB 3.0 Host Controller Logic
  - USB 2.0 and SuperSpeed Links Coexist in USB 3.0
  - USB 3.0 Composite Cable
    - USB 2.0 Signal Set
    - USB 3.0 SuperSpeed Signal Set
    - VBus Power (Shared by 2.0 and SuperSpeed Interfaces)
  - Layered Protocol Model for USB 3.0 SuperSpeed Interfaces
    - Application Layer
    - Protocol Layer
    - Link Layer
    - Physical Layer (PHY)
  - USB 3.0 Hubs
    - Hubs Connect Upstream at both USB 2.0 and SuperSpeed
    - Integrated 2.0 and SuperSpeed Hubs
    - Layered Protocol at Each SuperSpeed Hub Port
    - Packet Forwarding Responsibilities
  - Simple SuperSpeed Transaction Examples
    - IN Transaction
    - OUT Transaction
  - Link Level Error Handling
    - Header Packet (HP) Buffers at Link Layer
    - HP Replay on CRC Error
  - Link Level Header Packet Flow Control (Credit Based)
  - New Device Requests and SuperSpeed Descriptors
  - SuperSpeed Link Power Management Enhancements
    - Link Power Management
    - Function Power Management
- Features Introduced In USB 3.1
  - Enhanced SuperSpeed Host Controller Logic
  - Protocol Layer Changes
    - Type 1 and Type 2 Packet Priority
    - Transaction Ordering and Reordering
    - Transaction Packet (TP) Format Changes
    - Data Packet (DP) Format Changes
    - Isochronous Timestamp Packets (ITPs)
    - Link Management Packets (LMPs)
    - Precision Time Measurement (PTM)
    - Device Framework Changes
  - Link Layer Changes
    - Framing Ordered Sets
    - New *deferred* and *non-deferred* Data Packet Header *(DPH*)
    - Logical Idle
    - Link HP Buffers and Credit Based Flow Control Changes
    - Link Level Error Handling Changes
    - LTSSM and Link Training Changes
  - Physical Layer Changes
    - New Symbols/Ordered Sets
    - Low Frequency Periodic Signaling (LFPS) variants
    - Tx/Rx PHY Logical and Electrical Section Changes
  - USB 3.1 Hubs
    - SuperSpeedPlus Store and Forward Architecture
    - Improved Hub Buffering
    - Hub Arbitration of Upstream and Downstream Packets
    - SuperSpeed and SuperSpeedPlus Rate Matching

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Prerequisites: None, but some background in USB protocol is very helpful.

Course Material:

Students will be provided with an electronic version (PDF) of the slides used in this one-day course.