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USB 3.2 with xHCI Fundamentals

Training

Let MindShare Bring "USB 3.2 with xHCI" to Life for You

Each generation of the USB is backward compatible and a USB 3.2 topology may include devices operating at USB 2.0 Low Speed (LS), Full speed (FS), and High Speed (HS) as well as USB 3.x SuperSpeed (SS) Gen 1 and Gen 2. Prior to USB 3.2, USB cables, plugs, and receptacles were based on single-lane serial bus communications with an independent set of signals for USB 2.0 and SS Gen 1/Gen 2 communications. USB 3.2 adds an option for doubling the bandwidth of single-lane 5 Gb/s SS Gen 1 or 10 Gb/s SS Gen 2 by employing the extra Tx/Rx signal pair already present in USB Type-C (USB-C) interfaces. The result: a dual-lane SS Gen 1 or Gen 2 interface (referred to in the USB 3.2 Specification as Gen 1x2 or Gen 2x2, respectively). In this scheme, data is alternately "striped" across two lanes and sent in parallel—it effectively doubles bus bandwidth for a given clock speed. The peak transfer rate under USB 3.2 is now Gen 2x2: 10 Gb/s x 2 lanes = 20 Gb/s. Note that traditional single-lane SS Gen 1 (Gen 1x1) and SS Gen 2 (Gen 2x1) are still available and that the scheme has no impact on legacy USB protocol on the USB 2.0 signals.

In addition to the new Enhanced SuperSpeed (ESS) Gen 1x2, Gen 2x2 features, USB 3.2 carries forward the many SuperSpeed protocol optimizations first introduced in USB 3.0/USB 3.1 and designed to mitigate some of the disadvantages of USB 2.0 bus operations. These include unicast instead of broadcast packets, device asynchronous messages, packet bursting, end-to-end and link level flow control, link level error handling, link-level power management, and many others. Several significant enhancements to SuperSpeed Plus (SSP) hubs have also been added in the USB 3.2 specification. All of the above topics are covered in the USB 3.2 part of the class.

All generations of USB rely on platform host controllers to manage devices attached to each bus instance. USB 2.0 employed UHCI/OHCI and EHCI compliant host controllers to handle low, full, and high speed devices. The advanced capabilities of USB 3.x require new generations of USB host controllers. Course topics on the last day include Intel's eXtensible Host Controller Interface (xHCI). A single host controller based on xHCI can manage both USB 2.0 and Enhanced SuperSpeed (ESS) topologies as well as attached devices of any USB speed. The xHCI operational model, software interface (registers, memory data structures), doorbell-based work notification, and hardware transaction scheduling are all described.

Who Should Attend?

This five-day course is designed with hardware, software, and validation engineers in mind. Features and limitations of each generation of USB are described as is the role of xHCI compliant host controllers in managing attached devices and hubs.

Course Length: 5 Days

Course Outline:

Comprehensive USB 3.2

- Background
  - USB 2.0 Introduction and Protocol Limitations
  - USB 3.0 SuperSpeed Baseline Feature Set
  - USB 3.1 Enhancements
- USB 3.2 Introduction
  - New Feature List
  - USB 3.2 Platform Elements
    - Hosts
    - Hubs
    - Peripherals
  - USB 3.2 SuperSpeed Interface Basics
    - Dual-Simplex connection
    - Packet Based Protocol
    - Signals: x1 and x2 Links

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- End-to-End Protocol
  - SS Gen 1 End-to-End Protocol
    - Introduction to Protocol Layer Packets
    - SS Gen 1 IN/OUT Transactions
    - SS Gen 1x2 Link Impact on End-to-End Protocol
  - SS Gen 2 End-to-End Protocol Changes
    - Three Key Gen 2 Enhancements
    - SS Gen 2x2 Link Impact on End-to-End Protocol
- Port-to-Port Protocol
  - SS Gen 1 Port-to-Port Protocol
    - LTSSM and ESS Link States
    - Link Traffic Overview
    - Header Packet Processing
    - Header Packet Flow Control
    - Packet Acknowledgement and Retry
  - SS Gen 2 Port-to-Port Protocol Changes
    - Key Changes
    - SS Gen 2x2 Link Impact on Port-to-Port Protocol
- Chip-to-Chip Protocol
  - SS Gen 1 Chip-to-Chip Protocol
    - SS Gen 1 Tx PHY Logic
    - SS Gen 1 Rx PHY Logic
  - SS Gen 2 Chip-to-Chip Protocol Changes
    - The Big Differences
    - SS Gen 2x2 Link Impact on Chip-to-Chip Protocol
- ESS Link Reset Events
  - Power On Reset
  - Warm Reset
  - Hot Reset
  - Reset Propagation
- Link Training and Recovery/Retraining
  - SS Gen 1 Link Training
    - LTSSM States For Link Training
    - SS Gen 1 Logic To Be Trained
    - SS Gen 1 Link Training Sequence
    - SS Gen 1x2 Impact on Link Training
  - SS Gen 1 Link Recovery/Retraining
    - Motivation for Recovery
    - Rx Logic Requiring Retraining
    - LTSSM States For Recovery/Retraining
    - SS Gen 1 Recovery/Retraining Sequence
    - SS Gen 1x2 Impact on Link Recovery/Retraining
  - SS Gen 2 Link Training Differences
    - Overview of SS Gen 2 Link Training
    - SS Gen 2 Link Training Sequence
    - SS Gen 2x2 Impact on Link Training
  - SS Gen 2 Link Recovery/Retraining Differences
    - SS Gen 2 Recovery/Retraining Sequence
    - SS Gen 2x2 Impact on Link Recovery/Retraining
- Enumeration and Configuration
  - ESS Device Configuration Overview
  - When Attachment is Detected
  - USB 3.2 ESS Descriptors
- ESS Power Management
  - Link Power Management
  - Function Suspend
  - Function Wake
- USB 3.2 Hubs
  - USB 3.2 Hub Key Features
  - Deferred Transactions
  - SS Hub Architecture
  - SSP Hub Architecture

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eXtensible Host Controller Interface (xHCI) for USB

- Overview of xHCI
  - Motivations and Goals
  - Dual Bus Topology
  - xHC Implementation Options
  - Root Hub Ports
- xHCI Resources, Big Picture
- xHC Internal Registers
  - PCI Configuration Registers
  - MMIO Registers
- xHCI Memory Data Structures
  - Slot IDs, Doorbells, and Scheduling
  - Command Ring
  - Event Rings
  - Device Context Data Structure
  - Transfer Rings
- xHCI Interrupts
  - Interrupters and Event Rings
  - MSI-X Configuration
  - Interrupt Moderation
- xHC Reset & Initialization
  - Host Controller Reset Types
  - Host Controller Initialization
- Device Attachment & Initialization
  - Root Hub Port Status Change
  - *Enable Slot & Address Device* Commands
  - Device Context Setup
  - Configuration Selection

Appendices

- A: SuperSpeed (SS) Packet Formats
- B: ESS Bulk EP Streaming and UAS
- C: Latency Tolerance Message (LTM)
- D: ESS Signaling
- E: USB Type-C & Power Delivery Overview

Recommended Prerequisites: background in USB 2.0 protocol is very helpful.

Course materials:

Students will be provided with:

1. An electronic (PDF) version of the presentation used in class
2. An eBook (PDF) copy of MindShare's ***USB 3.0 Technology*** book by Don Anderson and Jay Trodden

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