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USB4 Architecture

Training

Let MindShare Bring "USB4 Architecture" to Life for You

Universal Serial Bus (USB) remains the most widely used cabled IO bus and is found in systems ranging from embedded controllers to workstations and servers. While USB 3.2 is the latest specification version for generic USB 2.0 and Enhanced SuperSpeed (ESS), the addition of USB4 introduces an entirely new capability--interleaved USB 3.2, PCI Express (PCIe), and DisplayPort (DP) packets on the multi-protocol USB4 link. One of the most important use cases for multiplexed IO protocols over a single bus applies to laptops, notebooks, tablets, and other small form factors where space is limited for both internal peripherals and external IO connectors. In this scenario, a USB4 dock may be connected to the host; downstream of the dock may be native protocol PCIe, USB 3.2, and DisplayPort peripherals: SSD, GPU, LAN adapter, multiple displays, etc. If a dock isn't needed, a USB4 port can be dedicated to a high bandwidth peripheral or charging power.

USB4 employs an enhanced version of Intel's Thunderbolt 3 *packet tunneling* scheme to support multiple protocols on a physical interface based on USB-C defined connectors, cables, and power delivery (USB PD). The USB-C connection used by USB4 also supports the backward compatibility required if native USB 3.x, USB 2.0, or DisplayPort alternate mode devices are attached to USB4-capable USB-C ports.

This 4-day course is a top-down, detailed look at USB4—including the roles played by two enabling specifications: *USB Type-C Cable* and Connector and *USB Power Delivery*. The first day of training presents an overview of key topics, many of which are covered in more detail in days 2-4. For those just needing an introduction to the major features of USB4, day 1 will provide it. Most of the same overview content is also available in a separate 1-day MindShare course entitled *USB4 Fundamentals.* Note that low-level details about native USB 3.2, PCIe, and DisplayPort protocols are not covered in this class. However, MindShare does offer in-depth courses on individual bus architectures, including both USB 3.2 and PCIe. For details on training options, visit our website or contact us directly.

You Will Learn

- USB4 fabric elements: hosts, hubs, and devices as well as their internal architectures
- USB4 link and its USB-C defined receptacles, plugs, and signal groups
- Passive/active cables and re-timers
- USB and DisplayPort backward compatibility requirements for USB4 hosts, hubs, peripherals
- The layered USB4 protocol
- USB4 host interface and connection manager role
- Tunneled packets, control packets, link management packets
- Per-link and end-to-end flow control
- Quality of Service
- Link error handling
- Link power management
- Physical layer (logical and electrical sections)
- USB4 link initialization and training sequence
- Configuration spaces and enumeration
- Other USB4 features: time synchronization, host-to-host communications

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Who Should Attend?

The full course is designed for hardware, software, and validation engineers requiring detailed USB4 coverage. The first day provides an overview which is suitable for those needing just an introduction to key USB4 concepts.

Course Length: 4 Days

Course Outline:

- USB4 Overview (Day 1 Content)
  - USB4 Motivations, Goals, Key Specifications
  - Dual-bus System Architecture: USB4 plus USB 2.0
  - Fabric Elements: Hosts, Hubs, Devices
  - USB4 Router and Adapter Architecture
  - Router Bypass Paths
  - USB4 View of USB-C Port Logic, Signal Groups, and Cables
  - Layered Protocol Overview
  - Transport Layer Packet Types and Routing Concepts
  - USB4 Configuration Spaces
  - Host Interface and Configuration Manager Roles
  - Brief Introduction to USB4 Physical Layer (Logical and Electrical Sections)
- Transport Layer Details
  - Packet Types, Formats, and Usage Models
    - Tunneled Packets
    - Control Packets
    - Link Management Packets
    - Idle Packets
  - Maximum Packet Sizes, Padding, Inter-packet Gap
  - Routing
    - Adapter Numbering
    - Router Numbering
    - HopID Packet Steering
    - Routing Tables
  - Quality of Service (QoS)
    - Ordering Rules: Single vs. Multiple Path
    - Link Level Flow Control: Buffers and Credits
    - Example: Packet Flow and Credit Updates
    - Egress Adapter Packet Arbitration & Scheduling
    - Connection Manager Path Tear-down

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- Packet Tunneling
  - Tunneling Support Requirements for Hosts, Hubs, Devices
  - PCIe Tunneling
    - PCIe Tunneled Traffic: TLPs, DLLPs, Ordered Sets, Out-of-Band (OOB) events
    - PCIe Adapter Requirements for TLP and DLLP Encapsulation
    - PCIe Adapter Requirements for Ordered Sets: TS, EIOS, EI, PERST
    - Handling PCIe Hot Plug
    - Handling Internal PCIe Ports
    - PCIe Precision Time Management (PTM) Considerations
    - PCIe Tunneling Example
  - USB3 Tunneling
    - USB3 Tunneled Traffic: LFPS, OS, Link Commands, LMPs, TP, ITP, DP
    - USB3 Adapter Requirements for LFPS and OS Encapsulation
    - USB3 Adapter Requirements for Link Command, TP, DP Encapsulation
    - Handling USB3 PM Transitions, Bandwidth Negotiation
    - Bandwidth Negotiation Events
    - Handling Internal USB3 Device
    - USB3 Tunneling Example
  - DisplayPort (DP) Tunneling
    - DP Adapter Protocol Stack
    - DP Adapter State Machine
    - DP Tunneled Packet Formats for AUX Path and Main-Link Path Packet Types
    - DP Tunneling Example
- Host Interface
  - Host Interface Adapter Implemented In Host Router
  - Provides Connection Manager Access to USB4 Fabric (Tunneled & Control Packets)
  - Host Interface May Be PCIe Based
  - Transmit (Tx) and Receive (Rx) Rings in Memory Used to Queue Fabric Traffic
  - One Tx/Rx Ring for Each USB4 Fabric Path (HopID 0 to HopID n)
  - Tx/Rx Descriptor Ring Modes: Raw and Frame
  - Host-to-Host Transaction Support
  - Interrupts
    - PCIe-Based Host Routers support both MSI/MSI-X and INTx
    - Tx and Rx Descriptor *Interrupt Enable* bit used to trigger interrupt upon completion
    - Number of Vectors: MSI (1 max), MSI-X (16 max)
    - Interrupt Moderation (Limits Rate of Interrupt Delivery to Host)
  - Programming Interface (*Assumes Host Interface Adapter Layer is PCIe based)*
    - PCI Space Base Address Register (BAR) tracks MMIO/ main memory blocks
    - Interrupt Management

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- Configuration Layer Details
  - Domains: Six Levels for Host and Device Routers (Depth 0 to Depth 5)
  - USB4 Router Topology IDs (7 Adapter Numbers in Route String Format)
  - Control Packets
    - Control Packet Payload
    - Read Request/Response Formats
    - Write Request/Response Formats
    - Notification Packet/Response Formats & Event Types
    - Hot Plug Event Packet Format
    - Inter-Domain (Host-to-Host) Request/Response Packet Formats
    - Control Packet Routing Example
- Physical Layer (Logical Section)
  - Sideband (SB) Channel Communications & Management
  - USB4 Link Initialization
  - Inbound and Outbound Transport Layer Packet Processing
  - Clock Compensation: Skip OS Insertion/Removal
  - De-skew Requirements
- Link Initialization and Training (5 Phases)
  - Phase 1: Initial Conditions (USB-C and USB Power Delivery Specifications)
  - Phase 2: USB4 Router Detection
  - Phase 3: Determination of USB4 Port Characteristics
  - Phase 4: Lane Synchronization & Training Start
  - Phase 5: USB4 Link Equalization
- USB4 Lane Adapter State Machine (per lane)
  - Lane Adapter State Machine States
  - Training Ordered Sets
- Other USB4 Topics
  - Time Synchronization
  - Physical Layer (Electrical Section)
  - USB4 and Thunderbolt 3 Interoperability

Recommended Prerequisites

Some background in USB, PCIe, or Thunderbolt protocols is very helpful.

Course Material:

Downloadable PDF version of the presentation slides