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x86 Architecture Programming

Let MindShare Bring the "x86 Architecture" to Life for You

This course teaches the x86 architecture (both 32-bit and 64-bit) through a mix of lectures and hands-on programming labs. All topics are explained in lecture format first and then the students are given programming labs in Assembly Language to reinforce the concepts and to get hands-on experience working with x86 processors at a very low level. This course focuses mainly on the behavior of Legacy Protected Mode, Compatibility Mode and 64-bit Mode as these are the modes most commonly used in modern operating systems.

The lab exercises range from printing to the screen using the flat memory model in legacy Protected Mode to setting up an interrupt driven, multitasking 64-bit Mode environment, with paging turned on.

You Will Learn:

- x86 programming basics like an overview of the instruction set, register set and operating modes
- The behavior of segmentation, how it was originally intended to be used and how it is actually used by operating systems today
- How to setup system calls using multiple methods (and what are benefits / side-effects of each)
- How to setup interrupt service routines for both software and hardware interrupts and implement a rudimentary scheduler
- How to implement paging in both the 32-bit environments as well as the 64-bit environments including using various page sizes

Course Length: 5 Days

Who Should Attend?

This course is ideal for software developers wanting to learn the x86 architecture in a hands-on environment.

Course Contents:

- **x86 Overview**
  - x86 ISA Background
  - x86 Instruction Set
  - Register Set & Address Spaces
  - Operating Modes
- **Segmentation**
  - Segment Registers (CS, SS, DS, ES, FS, GS)
  - Segment Descriptors
  - Global Descriptor Table
  - Local Descriptor Tables
  - Privilege Levels
- **Control Transfers**
  - Far Jumps and Calls
  - Call Gates
  - Optimized system calls (SYSENTER/SYSEXIT and SYSCALL/SYSRET)
  - Automatic Stack Switching
- **Task Management**
  - Task State Segments
  - Software Task Switching
  - Hardware Task Switching
    - Task Gates

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- **Interrupts and Exceptions**
  - Software and Hardware Interrupts
  - x86 Exceptions and their classifications
  - Interrupt Gates and Trap Gates
  - Interrupt Descriptor Table
  - Interrupt Stack Management
- **Paging**
  - Purpose
  - Basic Virtual-to-Physical Address Translation
  - Page Size Extensions
  - Physical Address Extensions
  - Translation-Lookaside Buffer (TLB) Management
- **Long (IA32e) Mode**
  - Long Mode Paging
  - Long Mode Segmentation
  - Long Mode Control Transfers
  - Long Mode Task Management
  - Long Mode Interrupt Handling
- **IO Accesses**
- **Instruction Prefixes**
- **Mode Switching**
  - Real Mode → Protected Mode
  - Protected Mode → Long Mode
  - 64-bit Mode ←→ Compatibility Mode
- **Debug Features**
- **Virtual-8086 Mode (VM86)**

Recommended Prerequisites:

Some experience with x86 Assembly Language is recommended.

Course Material:

MindShare will supply a hardcopy and electronic version of the presentation slides including the lab descriptions. MindShare also provides the SW tools and environment needed for the labs. Students are only required to bring an x86-based PC.

MindShare's ***x86 Instruction Set Architecture*** Book or eBook.
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