Last updated on: Sept 12, 2004

The Unabridged Pentium 4, First Edition Errata

Page	Severity	Date	Description
557	minor	8/31/04	In figure 24-3, change the bit numbers above the PDPT Index field from • "31 32" • to "31 30"
560	minor	8/31/04	In figure 24-6, change the bit numbers above the PDPT Index field from • "31 32" to "31 30"
564	minor	8/31/04	In figure 24-10, change the bit numbers above the PDPT Index field from • "31 32" to "31 30"
565	minor	8/31/04	In figure 24-11, change the bit numbers above the PDPT Index field from • "31 32" to "31 30"
802	trivial	8/31/04	Change heading • "Memory Type When Page Definition and MTTR Disagree" • to "Memory Type When Page Definition and MTRR Disagree"
887	minor	8/31/04	In figure 37-3, change the text note on the right side from • "All processors toggle BIST until BIST completed" • to "All processors toggle BNR# until BIST completed"
1084	trivial	8/31/04	In the sentence immediately preceding the second code fragment, • "(first implemented in the Pentium 4)" • should read "(first implemented in the Pentium III)".

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1113	Clarification	8/31/04	Add the following text: **A Cautionary Note** If a logical processor is in the MWAIT state and an interrupt or a task switch should occur, the subsequent execution of the iret instruction or a switch back to the task resumes execution with the instruction that immediately follows the MWAIT instruction. For this reason, the code that immediately follows the MWAIT instruction should test the sync variable to determine if it was actually written to. If it wasn't, the program should jump back to the MWAIT.

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1239	Clarification	8/31/04	Add the following text: **An Interesting Scenario** • Processor A experiences a cache miss in WB memory and starts a read transaction on the FSB. • Processor B has a copy of the line in the E state. It asserts HIT# in the Snoop Phase and changes the state of its line to the S state. • Because the memory read may take a while (e.g., the memory bus may be in use by the graphics adapter or by a PCI Express device adapter), the memory controller defers the read (and remembers snoop result). • The code executing on processor B has a store hit on its S copy of the line. • As a result, it initiates a kill transaction (i.e., a 0-byte Memory Read and Invalidate) to kill the copy of the line in processor A's cache. • Because the memory controller is currently fetching the line from memory for processor A, the memory controller issues a Retry Response to the kill. • The memory controller performs a Deferred Reply transaction to return the requested line to processor A. In the Snoop Phase, the memory controller asserts the HIT# signal (the "remembered snoop result from the initial read transaction that was deferred). • Processor A places the line in its cache in the S state. • Processor B retries the kill transaction and successfuly kills processor A's copy of the line. • Processor B stores into its S copy of the line and transitions it to the M state.

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1286	minor	8/31/04	In table 52-1, in last row change • "ADS# is deasserted during the packet B transmission." • to "ADS# is deasserted during the second BCLK of the transaction."
1315	minor	8/31/04	In the PM[5:4]# row of table 55-1, change "BPM4#" to "PM4#, and change "BPM5#" to PM5#".
1427	minor	8/31/04	In 5th major buller item, remove "64 byte line size" from end of the line.
1469	important	8/31/04	With reference to the bulleted item, it has come to the author's attention that, contrary to Intel's documentation, some processor implementations may save the processor's register set in starting at different addresses in SMM.
1470	important	8/31/04	The same issue described in the previous row of this table also applies to figure 60-1.
1506	minor	8/31/04	In Figure 61-5, change • "IO xAPIC is embedded in MCH" • to "IO xAPIC is embedded in ICH"
1550	minor	8/31/04	In the P5 column of the Illegal Register Adress row, change • "Y" • to "N"
1569	minor	8/31/04	In 1st bullet item, change • "(RT register 0 is associated with input 1, RT register 1 is associated with input 1, etc.)" • to "(RT register 0 is associated with input 0, RT register 1 is associated with input 1, etc.)
1570	important	8/31/04	On 1st text line, change • "via RT register 2 in the IO APIC" • to "via RT register 3 in the IO APIC"

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1570	important	8/31/04	In items 2 and 3, change • "RT register 2" • to "RT register 3"
1571	important	8/31/04	In item 12, change • "Normal Response" • to "No Data Response".
1571	important	8/31/04	In item 13, change • "RT entry 2" • to "RT entry 3"
1571	minor	8/31/04	In 1st bullet item, change • "(RT register 0 is associated with input 1" • to "(RT register 0 is associated with input 0"
1571	important	8/31/04	In the 3rd bullet item, change • "via RT register 2" • to "via RT register 3"
1571	important	8/31/04	In the 3rd line of item 2, change • "register 2" • to "register 3".
1571	important	8/31/04	In the last two indented bullet items on the page, change • "register 2" • to "register 3"
1572	important	8/31/04	In item 3, change • "register 2" • to "register 3"
1572	important	8/31/04	In item 12, change • "Normal Response" • to "No Data Response".
1572	important	8/31/04	In item 14, change • "register 2" • to "register 3"

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1573	important	8/31/04	In the last line of item 18, change • "on input 2" • to "on input 3"
1576	important	8/31/04	In the description of Redirection Table Register 0, change • "with IRQ input 1" • to "with IRQ input 0"
1576	important	8/31/04	In the description of Redirection Table Register 1, change • "with IRQ input 2" • to "with IRQ input 1"
1576	important	8/31/04	In the description of Redirection Table Register n, change • "with IRQ input n + 1" • to "with IRQ input n"
1586	important	8/31/04	Change the first sentence of the 3rd paragraph to read: "Table 61-9 on page 1587 and Table 61-10 on page 1588 describe the information that is output as the address and the write data in an interrupt transaction forwarded to the MCH by the ICH. "
1586	important	9/12/04	Strike the following sentence from the 3rd paragraph: "~~It should be noted that while this method is supported if a device adapter implements MSI-X capability, a device adapter that only supports MSI capability~~"
1587	trivial	8/31/04	In table 61-9, in the Redirection Hint bit description, in the 6th text line, add a close parentheses after "in this table)".

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1597	clarification	8/31/04	Add the following text: **Virtual Wire Mode** Prior to the enabling of the Local APIC, the processor's LINT0 input provides the same functionality as the old, legacy INTR input (this is referred to as PIC Mode). Interrupts from the legacy 8259A programmable interrupt controllers (PICs) are delivered to the processor on this pin and, in response, the processor generates the Interrupt Acknowledge transaction on the FSB to obtain the interrupt vector from the 8259As. Once the BSP's Local APIC has been enabled, legacy interrupts from the dual 8259As can be delivered in two ways (referred to as Virtual Wire Modes): • The processor's LINT0 pin van be programmed (via its LVT register) to deliver an ExtINT to the processor core when the LINT0 pin is asserted by the master 8259A. In response, the processor generates the Interrupt Acknowledge transaction on the FSB to obtain the interrupt vector from the 8259As. • A pin on the IO APIC can be programmed (via its respective RT register) to deliver an ExtINT to a processor when the IO APIC's respective input pin is asserted by the master 8259A. Upon receipt of the IPI message, the processor generates the Interrupt Acknowledge transaction on the FSB to obtain the interrupt vector from the 8259As.