Errata for PCIe 3.0 Book

November 12, 2017

Major Items

1. P104, Figure 3-9: the middle bridge on bus 6 should have a Subordinate Bus value of 9 instead of 8.

2. P144, 2nd paragraph, 5th line: "So to handle these cases, the limit register must be programmed with a higher value than the base." This, along with the description in this paragraph, is backward – the base must be programmed with a higher value than the limit to indicate an address range is not used.

3. P221, Table 6-2: Completion Header row shows the maximum calculation using 5DW when for Completion Headers, it should be 4DW. The correct maximum number of credits that can be advertised for Completion headers is 128 @ 4DWs = 2048 bytes.

4. P372, Figure 11-9: The byte striping example is incorrect based on the number of lanes specified. The characters for each lane should be:
   Lane 0: Character 0, Character 4, Character 8, Character 12
   Lane 1: Character 1, Character 5, Character 9, Character 13
   Lane 2: Character 2, Character 6, Character 10, Character 14
   Lane 3: Character 3, Character 7, Character 11, Character 15

5. P399, Table 11-3: the entry of 6ns for Gen3 is correct, but the clock period and number of clocks is not. The period at Gen3 is actually 1ns/clock instead of 1.25ns/clock, so the number of clocks is 6.

6. P427, 2nd paragraph, last sentence: "This example doesn't show it, but it's possible that a TLP might be incomplete at this point and would straddle the SOS by resuming transmission in the Data Block that must immediately follow the SOS." This sentence is incorrect and should be removed. As stated on page 429, "SOS's can still only be sent on packet boundaries…"

7. P503, Figure 13-38: the last bullet item says in L2 the receiver is in a high impedance state; this is incorrect and should state that the receiver must remain in a low impedance state in L2

8. P641, item 1 is incorrect and should say: "1. C_{-1} <= Floor (FS/4): In our case Floor (30/4) = 7. Thus, 3 <= 7 evaluates true."

9. P748, the three bullet items under the subtitle "Negotiation Required to Enter L1 ASPM" have the port directions backwards in the description. The bullets should say:

   - PM_Active_State_Request_L1 DLLP - issued by the downstream component (which is an upstream port) to start the negotiation process.

- PM_Request_Ack DLLP - returned by the upstream component (which is a downstream port) when all of its requirements to enter L1 ASPM have been satisfied.
- PM_Active_State_Nak message TLP - returned by the upstream component when it is unable to enter the L1 ASPM state.

10. P823, bit 15 description: When this bit is set, the description should read: “Function is **enabled** to use **MSI-X** to request service and won’t use MSI or INTx Messages.”

Minor Items

1. P9, 1st line and P10 1st line and P981: PCI stands for Peripheral Component Interconnect, not Peripheral Component Interface

2. P52, last paragraph says: “… thought was given to making it cable of operating as…” the word “cable” should be “capable”

3. P166, last sentence should start with “They” instead of “The”.